Thyristor-inserted MMC Sub-module Topology with DC Fault Blocking Capability

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***Abstract*—Modular multilevel converter (MMC) is increasingly being applied to high voltage direct current (HVDC) systems. However, dc short circuit situations restrain the application of a conventional half bridge MMC system. In this paper, a new sub-module topology with inserted thyristor can help the MMC system clear a dc side fault. Working states and devices voltage stress of the proposed topology are analyzed and the conduction loss comparison between the proposed topology with several existing topologies with dc fault blocking capability is carried out. Results show the proposed topology is superior to other topologies in terms of conduction loss while using the same voltage rating devices. Besides, compared with traditional half bridge topology, only thyristors and diodes are added in the proposed topology. Therefore, cost of the proposed topology can be lower than conventional hybrid MMC sub-modules. At last, the fault blocking capability of the proposed topology is verified in the simulation.**

***Index Terms*—Fault current limiting, high voltage direct current (HVDC) transmission, modular multilevel converter (MMC).**

I. Introduction

MODULAR multilevel converter (MMC) has become one of the most popular topologies used in high voltage direct current (HVDC) transmission systems [1]. Due to its high modularity and good scalability, MMC can easily find application in systems transmitting high-voltage and huge-power.

Nowadays, the most widely used MMC system is based on half-bridge sub-module (HBSM) due to its simple structure and high efficiency. However, there is a major challenge for MMC systems based on HBSM that a dc side fault may cause serious consequences in them [1]–[3]. Owing to the freewheeling diodes in the HBSM, ac side currents can directly go through the arms of MMC system, and inject into the dc side fault point, which may cause great overcurrent in the path they flow through. Overcurrent may not only destroy the semiconductor devices in the MMC system, but also influence stability of the ac side system.

Several kinds of methods to handle the problem caused by dc side fault in MMC systems have been proposed. The first method is by tripping the ac side circuit breakers to isolate ac side with MMC system [5]–[7]. Since there is no voltage source in the ac side anymore, overcurrent in MMC system can be suppressed.

The second method is by tripping the dc side circuit breaker [8], [9]. This method can directly separate the dc side fault point from the system, and the MMC system can then operate in dc side open circuit condition.

These two kinds of methods need extra components in the MMC system, that is, an ac and dc circuit breaker. Besides, if the circuit breaker is constructed only by conventional mechanical switches, extra bypass devices, typically thyristors, are needed to protect the semiconductors in the MMC system during the mechanical response time.

There is another method where no extra equipment is needed to block the dc side fault; that is, applying suitable MMC sub-modules (SMs) to construct the MMC system [2], [10]–[14]. These SMs can block a dc fault through a certain control strategy and are known as "sub-modules with dc fault blocking capability".

In high voltage MMC systems, owing to the number of sub-modules in one arm is very large, the switching frequency can be quite low. Therefore, the major factor of loss is conduction loss [15]. However, sub-modules have a common point that there are more conducting semiconductors in normal state than half-bridge sub-module, which will lead to higher conduction loss. How to equip the MMC system with dc side fault blocking capability, while maintaining relatively low conduction loss is a valuable research direction.

A novel MMC topology realizing dc side fault blocking based on thyristor is proposed in this paper. The thyristor-inserted topology can block a dc side fault while maintaining relatively low conduction among other topologies. In Section II, the principle of dc side fault blocking by using a sub-module is introduced. A voltage source equivalent circuit is then discussed, and the root cause why conventional topologies increase conduction loss is pointed out. In Section III, the thyristor-inserted topology is introduced, and its working states are analyzed. In Section IV, comparison between the proposed topology and existing topologies is conducted. DC side fault blocking capability of the proposed topology is verified by a simulation in Section V. Section VI concludes the paper.

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II. Principle of DC Fault Blocking Realized by MMC Sub-module

The mechanism of overcurrent in an HBSM-based MMC system in DC fault condition is briefly introduced in the introduction part. The fault blocking process has been analyzed in [1], [10].

Therefore, we will only focus on the requirement for sub-modules to block dc side fault.

Figures 1 and 2 illustrate two typical fault current loops in a half-bridge-based MMC system and full-bridge-based MMC system, respectively. As can be seen from the current path, 'Loop 1' can be cut off by IGBT, therefore, overcurrent caused by this loop can be easily handled. However, current in 'Loop 2' will flow through uncontrollable diodes, which will lead to overcurrent in half-bridge-based MMC system. In a full-bridge-based MMC system, current in 'Loop 2' will flow through capacitors in the sub-modules, which will lead the full bridge sub-module to output a negative voltage to cancel the ac sideline voltage. When the amplitude of negative voltage in the loop is large enough to fully cancel the ac line voltage, the fault current will be blocked.

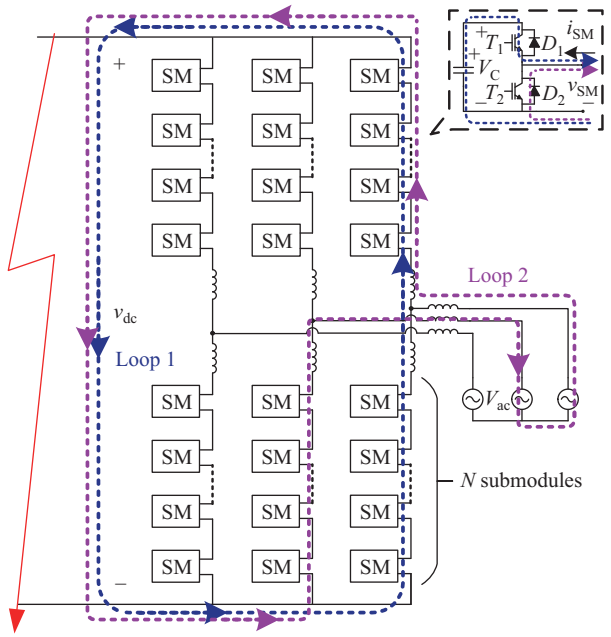

Fig. 1. Two possible fault current loops in half-bridge-based MMC system.

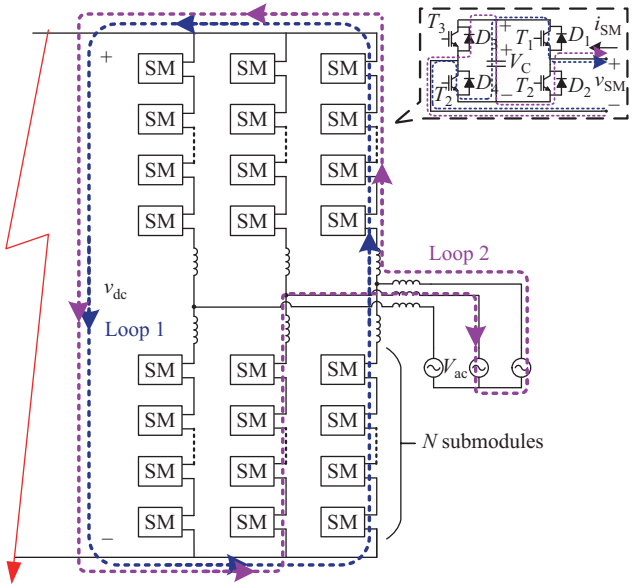

Fig. 2. Two possible fault current loops in full-bridge-based MMC system.

The principle of dc side fault blocking, realized by MMC sub-module, can then be derived. Consider the normal operation condition of half-bridge-based or full-bridge-based MMC system. Ignoring the voltage drop on the arm inductors, the following equations can be derived.

$$\sqrt{2}V_{\mathrm{ac}} = N \cdot V_{\mathrm{C}} \cdot \frac{m_{\mathrm{ac}}}{2} \tag{1}$$

$$V_{\mathrm{dc\_n}} = 2N \cdot V_{\mathrm{c}} \cdot \frac{1}{2} = N \cdot V_{\mathrm{c}} \tag{2}$$

where V_{ac} is the root mean square (RMS) value of ac side phase voltage; N is the number of half bridge sub-modules or the number of full bridge sub-modules in one arm; V_{C} is the average capacitor voltage in each sub-module; m_{ac} is the ac modulation ratio of converter system, which is usually less than 1; $V_{\mathrm{dc\_n}}$ is the nominal dc side voltage.

In dc side fault state, if the dc link residual voltage $V_{\mathrm{dc\_fault}}$ is known, the fault current is determined by the ac sideline-to-line peak voltage and the sub-module output voltage u_{SM}. Take loop 2 in Fig. 2 for example. The following equation can be deduced (also need to ignore the influence of arm inductors):

$$V_{\mathrm{dc\_fault}} = 2N \cdot u_{\mathrm{SM}} + \sqrt{2} \cdot \sqrt{3}V_{\mathrm{ac}} \tag{3}$$

In extreme conditions, residual voltage should be regarded as 0, which will determine the minimum amplitude of average negative voltage the sub-modules should output to block the fault, as is shown in (4).

$$u_{\mathrm{SM}} \leq -\frac{\sqrt{2} \cdot \sqrt{3}V_{\mathrm{ac}}}{2N} = -\frac{\sqrt{3}}{4} m_{\mathrm{ac}} \cdot V_{\mathrm{C}} \tag{4}$$

Define $\alpha = (\sqrt{3}/4) \cdot m_{\mathrm{ac}}$ ($m_{\mathrm{ac}} < 1$), then if the average negative output voltage amplitude of sub-modules in each arm can be greater than the maximum output voltage multiplied by α, the MMC system can block the dc side fault.

Check the principle derived above using the MMC system based on clamped double sub-module (CDSM) [2]. The operating states of CDSM are shown in Fig. 3.

As can be seen from Fig. 3, CDSM can output positive voltage up to $2V_{\mathrm{C}}$ in normal state. In dc side fault state, all switches of CDSM are turned off. The voltage output of CDSM is determined by current direction. If current is in the same direction as the reference current in Fig. 3, the current is positive, and the voltage is $2V_{\mathrm{C}}$, as is shown in Fig. 3(e). This state can block the current path 1 shown in Figs. 1 and 2.

Fault current in the ac current path is opposite the reference current in Fig. 3. Therefore, i_{SM} is less than 0 and the sub-module output a negative voltage with amplitude V_{C}. Since V_{C} is greater than $\alpha \times 2V_{\mathrm{C}}$, the dc side fault can be blocked. This fits the well-known understanding.

However, it can also be found from Fig. 3 that the IGBT module marked red is always in the normal current path, which

will lead to increase of conduction loss. Not only CDSM, but other topologies using conventional IGBT modules also share this problem. The extra switch in other topologies, which only serves as a current path decider, is marked red in Fig. 4. These

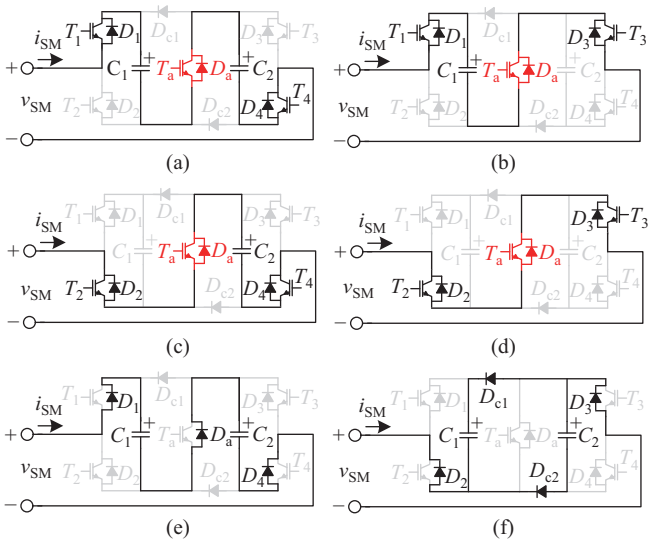

Fig. 3. Operating states of CDSM. (a) $v_{SM} = 2V_C$. (b) $v_{SM} = V_C$. (c) $v_{SM} = V_C$. (d) $v_{SM} = 0$. (e) $v_{SM} = 2V_C$. (f) $v_{SM} = -V_C$.

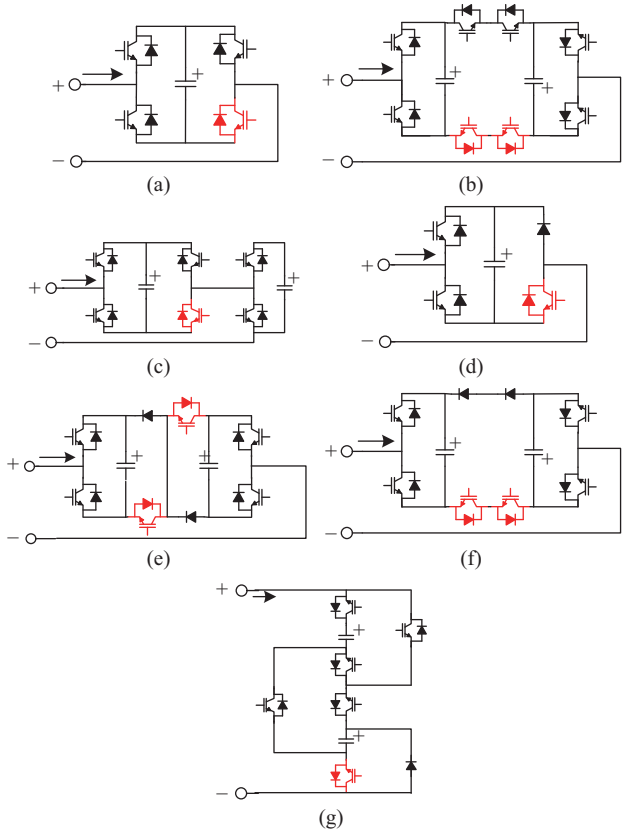

Fig. 4. Extra switches which lead to the increase of conduction loss in existing topologies. (a) Full bridge sub-module (FBSM) [3]. (b) Five-level cross connected double sub-module (CCDSM) [10]. (c) Mixed-cell sub-module [11]. (d) Unipolar-voltage full bridge sub-module (UFBSM) [8]. (e) Three level clamp-circuit-based sub-module (CCSM) [9]. (f) Serial connected double sub-module (SCDSM) [8]. (g) Switched capacitor submodule (SCSM) [12].

switches are always on during normal operation but will be turned off to change the current path in dc side fault state.

The root cause for the existence of these switches is that conventional IGBT module cannot block current flowing from the emitter side. Therefore, some method should be taken to block current in this direction. These sub-modules employ the extra IGBT modules to block the current, which lead to increase of conduction loss.

III. Thyristor-Inserted Sub-Module Topology and Its Operating States

To reduce conduction loss in sub-modules with dc side fault blocking capability, a new method should be taken. One plan is to adopt a new fully-controlled device that can directly block current from emitter side to construct the sub-module. Sub-modules constructed according to this idea are mentioned in [16], [17]. These sub-modules employ reverse-blocking IGBT (RB-IGBT) as the current path decider, and the number of semiconductors in the normal current path can be reduced, thus reducing conduction loss.

Another option is to choose a low conduction loss device to replace the extra conventional IGBT module in the normal current path. As is mentioned in the introduction part, thyristors are usually adopted to protect devices in the half bridge sub-module. The mechanism where thyristors can protect semiconductors is that thyristors have lower forward voltage than conventional IGBT and diode when conducting the same current. Therefore, using thyristor as the fault current blocker may be a good way to realize dc fault blocking while maintaining a relatively low conduction loss.

Based on the idea mentioned above, a novel sub-module topology using thyristor is proposed. As is shown in Fig. 5, the topology is based on two serial-connected half bridge sub-modules. The second half bridge is inserted with two pairs of anti-paralleled thyristors. Two freewheeling diodes are added to the circuit to conduct the fault current when the thyristors are blocked.

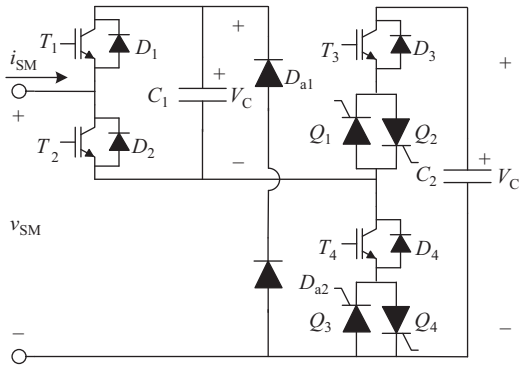

Fig. 5. Thyristor-inserted sub-module.

Normal operating states of this thyristor-inserted sub-module is shown in Fig. 6. Assuming voltages on capacitors C_1 and C_2 are both V_C, then the working states table can be deducted in Table I. In the working states table, '1' means the switch is driven to be in on-state. '0' means driving signal for

this switch is blocked. The polarity of current and voltage is referred to the reference direction shown in Fig. 6. '/' means no matter the current direction, the output of this sub-module is $v_{\rm SM}$.

Two dc side fault operating states of the proposed topology are shown in Fig. 7. In Fig. 7(a), corresponding to 'State 5' in Table I, although the gate drive pulse is removed, due to characteristics of the thyristor, if the forward current flows through the thyristor, the thyristor will continue freewheeling until the current drops to 0, then the thyristor will be blocked.

In Fig. 7(b), corresponding to 'State 6' in Table I, this state requires some special operations to ensure the thyristors will be turned off. The dc side fault blocking control strategy is shown in Fig. 8. The waveform $v_{\rm dc}$-t shows variation of dc link voltage with time. The waveform $S_{\rm fault}$-t shows the dc fault signal of the MMC system. If $S_{\rm fault}$ is 0, the control strategy of the system is normal state control strategy. If $S_{\rm fault}$ is 1, the system will work in dc side mode. The waveform of T_1&T_2-t shows the control signal of T_1 and T_2 in the MMC system. Since the first half bridge consists of T_1 and T_2, they work in complementary mode with dead zones. However, since it is not known what the operating state in Fig. 7 is, the switching state of T_1 and T_2 cannot be determined. Therefore, a rectangle with a diagonal fill indicates they are operating under normal conditions. If T_1&T_2 is 0, the driving signals of IGBTs T_1 and T_2 are removed. The waveforms of T_3-t and T_4-t have similar meaning. T_3 and T_4 also work in complementary mode with dead zones. The waveform of Q_1&Q_2-t shows the control signal of Q_1 and Q_2 in the MMC system. If Q_1&Q_2 is 1, the driving signals of thyristors Q_1 and Q_2 are applied; if Q_1&Q_2 is 0, the driving signals of thyristors Q_1 and Q_2 are removed. The waveform of Q_3&Q_4-t has similar meaning.

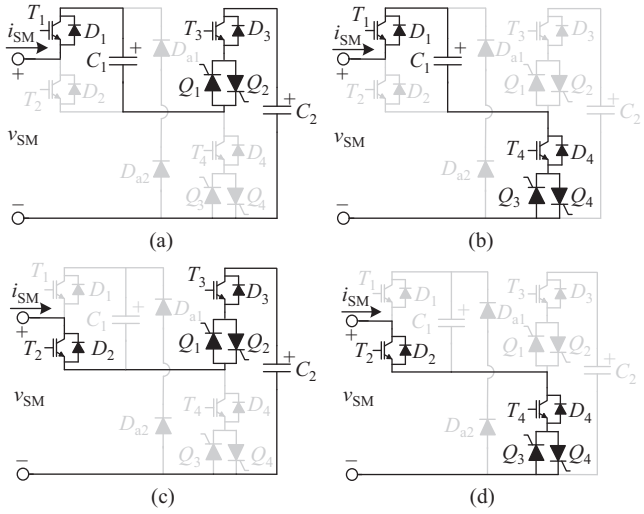

Fig. 6. Normal operating states of thyristor-inserted sub-module. (a) $v_{\rm SM} = 2V_{\rm C}$. (b) $v_{\rm SM} = V_{\rm C}$. (c) $v_{\rm SM} = V_{\rm C}$. (d) $v_{\rm SM} = 0$.

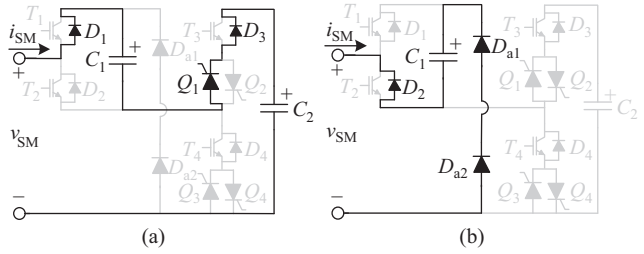

Fig. 7. DC side fault operating states of thyristor-inserted sub-module. (a) $v_{\rm SM} = 2V_{\rm C}$. (b) $v_{\rm SM} = -V_{\rm C}$.

TABLE I
WORKING STATES OF THE PROPOSED TOPOLOGY

State	T_1	T_2	T_3	T_4	Q_1&Q_2	Q_3&Q_4	$i_{\rm SM}$	$v_{\rm SM}$
1	1	0	1	0	1	1	–	$2V_{\rm C}$
2	1	0	0	1	1	1	–	$V_{\rm C}$
3	0	1	1	0	1	1	–	$V_{\rm C}$
4	0	1	0	1	1	1	–	0
5	0	0	0	0	0	0	>0	$2V_{\rm C}$
6	0	0	0	0	0	0	<0	$-V_{\rm C}$

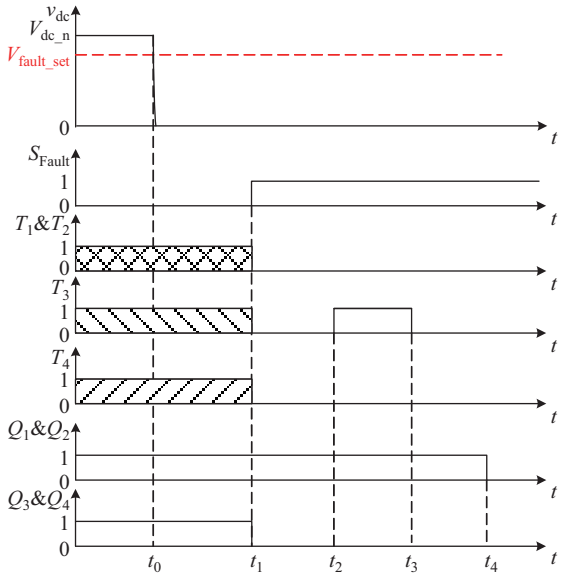

Fig. 8. The dc side fault blocking control strategy.

Before t_0, the MMC system based on the proposed topology works in normal state. Voltage of dc link is $V_{\rm dc\_n}$. At t_0, the MMC system meets with a dc side fault. The dc side voltage starts to drop and current started to flow to the dc fault point. At t_1, the fault is detected due to the fault detecting delay. The $S_{\rm fault}$ signal is immediately set and all IGBTs are turned off. The driving pulses for Q_3 and Q_4 are also removed immediately. After a small delay, at t_2, the driving signal for T_3 is applied to force thyristor Q_3 to turn off. At t_3, the driving signal of T_3 is removed. At t_4, driving pulses for Q_3 and Q_4 are removed to share voltage stress on the IGBT module T_3. In the recovery process, the driving signals of Q_3 and Q_4 are first applied. If no overcurrent occurs, it means the dc side fault is cleared, and the driving signals of Q_1, Q_2 and the enable signal of all IGBTs can then be applied. If overcurrent occurs, driving pulses for Q_3 and Q_4 are removed and Q_1, Q_2 and T_3 are turned on to apply a reverse voltage on Q_3 to force it off.

Since the thyristors are all serially connected with IGBTs in the proposed topology, and the gate pulse for the thyristors are always applied to ensure they are in on-state in normal operation state, the switching process of the arm will be

controlled by the IGBT. In [1], the authors have proved that a hybrid series connection can be applicable to dc choppers in high-voltage and high-power applications.

If the current-rising-rate of the thyristor needs to be limited, then a snubber circuit for IGCT [18] can be used in this circuit, as is shown in Fig. 9. In this way, the circuit will greatly improve the robustness at the cost of a slight increase in the loss.

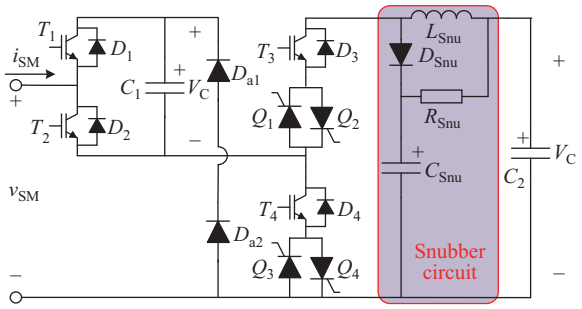

Fig. 9. Proposed sub-module with current-rising-rate limiter.

IV. Comparison Between Existing Topologies

After analyzing the working states of the proposed topology, comparison between existing topologies with dc side fault blocking capability and the proposed topology can be analyzed.

Cost and loss are always problems to be considered in the construction of converter systems. Since the capacitors of the proposed topology can be the same as with existing topologies, the difference in cost is mainly dependent on the semiconductor devices. Factors that influence the cost of semiconductor devices are quantity, rating and type. The quantity and type of semiconductors can be easily found in the topology. Therefore, only rating of the semiconductor devices should be analyzed.

Since the proposed topology keeps all thyristors on in normal operation state and the thyristors are serially-connected to the IGBT modules, switching transition voltage will only be applied on the IGBT and diode. Therefore, the serially connected thyristors will not increase switching loss. Besides, as is mentioned in the introduction part, in HVDC-MMC systems, there are hundreds of sub-modules in one arm, making the switching frequency quite low. Switching loss is not the major part of loss. So, only conduction loss is analyzed in detail in this section.

A. Voltage Stress Analysis

Voltage stress of the proposed topology can be analyzed in four loops as is shown in Fig. 10. In Fig. 10(a), T_1, D_1, T_2, D_2 and C_1 form a closed loop. Therefore, voltage on the semiconductors will not exceed voltage on C_1. From Fig. 10(b) and Fig. 10(d), voltage stresses on T_4, D_4, Q_3, Q_4, D_{a1} and D_{a2} can be derived. Voltage on T_4, D_4, Q_3 and Q_4 will not exceed the maximum voltage on C_1 or C_2, and voltage on the combination of D_{a1} and D_{a2} will not exceed the sum of voltage on C_1 and C_2. From Fig. 10(b) and Fig. 10(c), voltage on T_3, D_3, Q_1 and Q_2 can be derived. Voltage on the

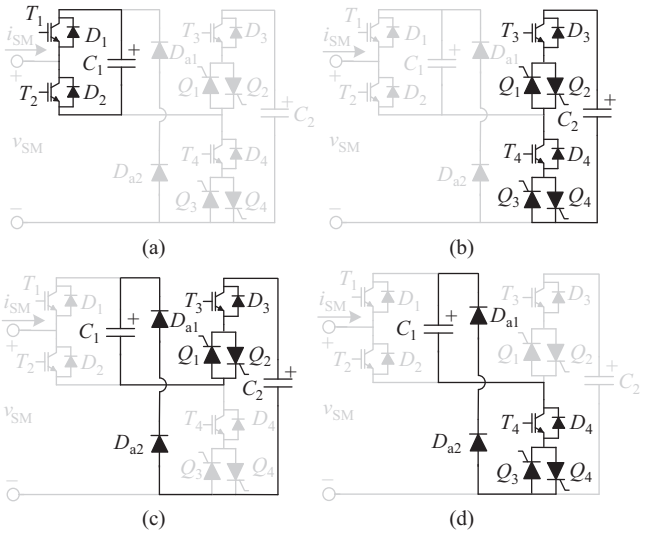

Fig. 10. Four loops for analyzing the voltage stress. (a) Loop 1. (b) Loop 2. (c) Loop 3. (d) Loop 4.

combination of D_3 and Q_1 will not exceed the sum of voltage on C_1 and C_2.

If the maximum voltage on C_1 and C_2 is represented as v_{maxC1} and v_{maxC2}, and proper balancing circuits are applied to all serially connected devices, voltage stress on all devices will not exceed the larger of v_{maxC1} and v_{maxC2}. Therefore, the rating of all devices can also be the same as conventional existing topologies.

B. Conduction Loss Analysis

In this part, a relatively simple method is used to calculate conduction loss of the given sub-modules. The calculation method is chosen according to [20].

Taking the 3300 V/1500 A IGBT module FZ1500R33HL3 and 3600 V Thyristor module T901N36TOF of Infineon for conduction loss calculation. The forward voltage of IGBT, diode and thyristor can be represented by (5).

$$\begin{cases} v_{\mathrm{IGBT}}(i) = r_{\mathrm{IGBT}} \cdot i + V_{\mathrm{IGBT0}} \\ v_{\mathrm{diode}}(i) = r_{\mathrm{diode}} \cdot i + V_{\mathrm{diode0}} \\ v_{\mathrm{thyristor}}(i) = r_{\mathrm{thyristor}} \cdot i + V_{\mathrm{thyristor0}} \end{cases} \tag{5}$$

The calculation method of linear fitting coefficients of IGBT and diode can be found in [21], and the linear fitting coefficients of thyristor can be found in its datasheet. All coefficients listed in Table II are obtained at the junction temperature $T_{vj} = 125$ °C.

TABLE II
Loss Coefficients of the 3300 V/1500 A IGBT Module FZ1500R33HL3 and T901N36TOF of Infineon at $T_{vj} = 125$°C

Coefficient	Value	Coefficient	Value
r_{IGBT}	1.122 mΩ	v_{IGBT0}	1.459 V
r_{diode}	0.706 mΩ	v_{diode0}	1.175 V
$r_{\mathrm{thyristor}}$	0.413 mΩ	$v_{\mathrm{thyristor0}}$	1.000 V

From Table II, it can be found that the loss coefficients of thyristors are both the lowest one among the three types of

TABLE III
COMPARISON OF DIFFERENT MODULAR MULTILEVEL CONVERTER SUB-MODULE TO OUTPUT TWO LEVEL POSITIVE VOLTAGE

Item	HBSM	CDSM	FBSM	CCDSM	Mixed-cell SM	UFBSM	CCSM	SCDSM	SCSM	Thyristor-inserted SM
Number of IGBTs	4	5	8	8	6	6	6	6	6	4
Number of diodes	4	7	8	8	6	8	8	8	7	6
Number of capacitors	2	2	2	2	2	2	2	2	2	2
Number of thyristors	0	0	0	0	0	0	0	0	0	4
DC side fault blocking capability	Does not have	Has	Has	Has	Has	Has	Has	Has	Has	Has
Normalized conduction loss (*1)	1	1.413	1.826	1.826	1.413	1.826	1.826	1.826	1.413∼ 1.826 (*2)	1.306
Total cost of semiconductors	4.4	5.7	8.8	8.8	6.6	6.8	6.8	6.8	6.7	5.4

Note: (*1) The normalized conduction loss is the conduction loss of this topology normalized by the conduction loss of HBSM;
(*2) The average conduction loss of SCSM is greater than CDSM but lower than FBSM [12].

devices, no matter the equivalent resistance r or the threshold voltage V. Then, a qualitative way to understand the conduction loss of the proposed topology is lower than of existing topologies can be obtained by analyzing Fig. 4 and Fig. 6. In existing topologies, current will go through an extra diode or IGBT, but in the proposed topology, current will only go through an extra thyristor. Therefore, conduction loss is lower due to lower forward voltage.

A more detailed comparison table is shown in Table III. In Table III, all topologies can output two level positive voltages, which means two sub-modules are required for HBSM, FBSM and UFBSM while other topologies only need one sub-module to be taken into consideration. The number of semiconductor devices can easily be counted from the different topologies. Conduction loss can also be deducted from the method shown in the appendix with $m_{\rm ac} = 0.816$, $\cos(\phi) = 1$ and $I_{\rm dc} = 800$. To make the results intuitive, the conduction loss of all kinds of topologies are normalized by that of HBSM. It can be found from Table III that conduction loss of the proposed topology is lower than all existing topologies with dc side fault blocking capability listed in the table. Therefore, MMC systems based on the proposed topology has more advantages in conduction loss.

C. Cost Analysis

In this part, a cost evaluation method is chosen according to [22]. Also suppose if IGBT cost is 1, then thyristor is 0.2 and diode is 0.1. The total cost of each sub-module can also be found in Table III.

As can be seen from the result, the proposed topology has the lowest cost among those topologies with fault blocking capability. Therefore, the topology can be applied in the MMC system to reduce cost.

V. SIMULATION VERIFICATION

To verify the dc side fault blocking capability of the proposed topology, simulation of an MMC system based on the proposed topology is conducted in the MATLAB/Simulink environment. The nominal value of the system is shown in Table IV. To show the topology can both block a dc side fault in inverter mode and rectifier mode, both working modes are simulated.

System configuration is shown in Fig. 11. Polarity of all waveforms is given according to the reference direction in Fig. 11. Since power flow reference direction is from ac side to dc side, the active power P is positive in rectifier mode and negative in inverter mode. Inverter mode simulation results are shown in Fig. 12, and the rectifier mode simulation results are shown in Fig. 13.

TABLE IV
NOMINAL VALUE OF THE MODELED SYSTEM

Parameter	Value
Rated MMC dc side voltage	60 kV
Rated active power	±60 MW
RMS ac voltage (L-L)	30 kV
Number of SMs per arm	10
SM capacitor voltage	3 kV
Arm inductance	20 mH
AC side leakage inductance	2 mH
Arm resistance	0.015 Ω
Capacitance of each capacitor	10 mF
Switching frequency	1 kHz

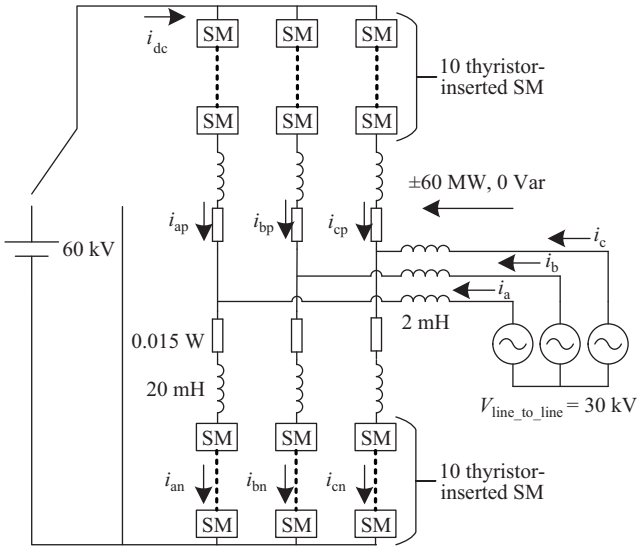

Fig. 11. System configuration in the MATLAB/Simulink environment.

To make the simulation closer to the actual system, fault detecting delay and control delay are added to the system, the fault operation strategy worked 100 μs later than the fault happened.

The dc side fault happens at $t = 0.511$ s. The dc side voltage directly drops to 0 at that point. After the fault is detected, as can be seen from Fig. 12(b), the dc side fault current is immediately restrained to 0, which means the dc side contact

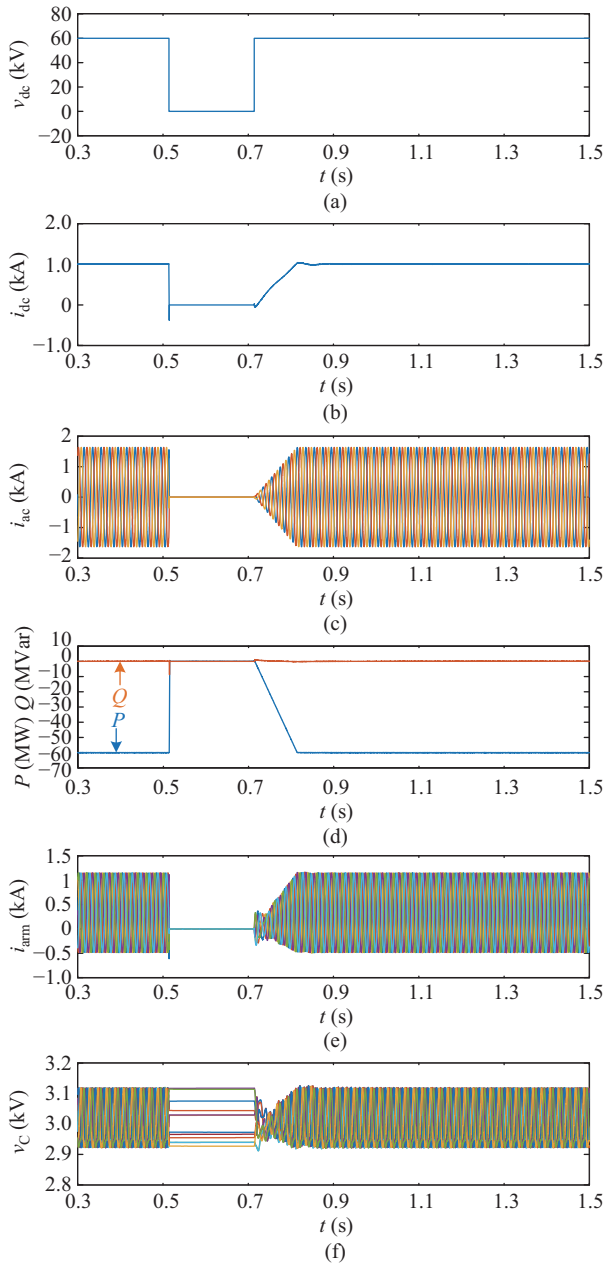

Fig. 12. DC fault blocking and recovery waveforms of the thyristor-inserted MMC system in inverter mode. (a) DC voltage. (b) DC current. (c) Three-phase current. (d) Active and reactive power. (e) Arm currents. (f) Capacitor voltages.

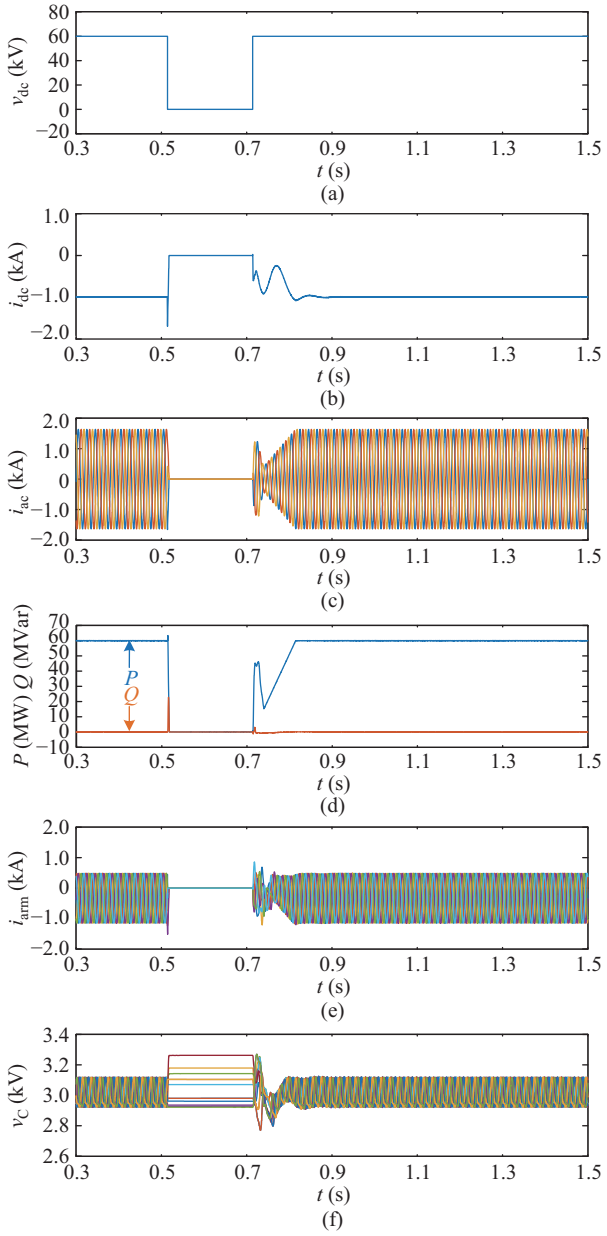

Fig. 13. DC fault blocking and recovery waveforms of the thyristor-inserted MMC system in rectifier mode. (a) DC voltage. (b) DC current. (c) Three-phase current. (d) Active and reactive power. (e) Arm currents. (f) Capacitor voltages.

switch can trip without arc. It will be very helpful for the HVDC transmission system with overhead line. Fig. 12(c) shows simulation results of the three phase currents in the modeled system. Three phase currents are restrained to zero soon after the fault is detected. Therefore, the ac grid will not suffer a three-phase short-circuit fault when there is a dc side fault. Fig. 12(d) shows simulation results of the active power and reactive power of the modeled system. Active power can gradually go back to the given value after the dc side fault. Fig. 12(e) shows simulation results of the arm currents of the modeled system. It can be easily found there is no overcurrent in each arm. Therefore, safe and reliable operation of the semiconductor devices can be guaranteed. Fig. 12(f) shows simulation results of the capacitor voltages in all arms. The capacitors will not suffer high voltage stress during the fault process and after the recovery process in inverter mode.

In Fig. 13, operation of the converter in rectifier mode is simulated. In Fig. 13(b), dc side overcurrent will be more severe than of the inverter mode due to current direction at the fault instant. Since the fault current direction is from ac side to dc side, the dc side current in rectifier mode will inevitably increase during the dc side fault. However, the fault current can be quickly restrained by applying the fault blocking strategy. In Fig. 13(c), the ac side overcurrent is also restrained to zero immediately. In Fig. 13(d), active power and reactive power of the rectifier MMC system are shown. A spike of reactive power can be found after the dc side fault. That is because of the fault

detecting delay set for the simulated system. In Fig. 13(e), a small overcurrent in arm currents can be observed, which is caused by two reasons. One is the fault detecting delay and the other is force commuting in control strategy. In Fig. 13(f), a more severe capacitor voltages overshoot can be observed due to large arm currents. However, the overvoltage amplitude does not exceed 10% of the nominal operation voltage, which can be withstood by the margin of the capacitors.

VI. Conclusion

A novel thyristor-inserted sub-module is proposed in this paper. It has dc side fault blocking capability. Besides, the proposed topology only increases the number of diodes and thyristors when compared to HBSM. Therefore, an MMC system based on the proposed topology can have 7.6% lower conduction loss and 18.2% lower cost than HBSM and FBSM hybrid MMC system. The dc fault blocking control strategy of the proposed topology is introduced and operation of the proposed topology is simulated in the MATLAB/Simulink environment. Results verify the dc side fault blocking capability of the proposed topology.

Appendix

For simplicity, a circulating current restraining control method is taken, and assuming the capacitor is large enough, the circulating current restraining control method caused little duty change on each sub-module. Therefore, phase A upper arm current waveform $i(t)$ and duty cycle $d(t)$ can be represented as (A1). The amplitude of fundamental frequency current can be obtained by the loss-free MMC converter model. Parameter $m_{\rm ac}$ represents the modulation ratio. The parameter $I_{\rm dc}$ represents the dc side current. The parameter $\cos(\phi)$ is the power factor of the converter system. The parameter f is the working frequency of the system.

$$\begin{aligned} i(t) &= I_{\rm dc}\cdot\left(\frac{1}{3}+\frac{2}{3m_{\rm ac}\cos(\phi)}\cdot\sin(2\pi f\cdot t+\phi)\right)\\ d(t) &= \frac{1}{2}-\frac{m_{\rm ac}}{2}\sin(2\pi f\cdot t) \end{aligned} \tag{A1}$$

From (A1), the current zero-crossing point can be derived.

$$\begin{aligned} t_1 &= \frac{1}{2\pi f}\left(\pi+\arcsin\left(\frac{m_{\rm ac}\cos(\phi)}{2}\right)-\phi\right)\\ t_2 &= \frac{1}{2\pi f}\left(2\pi-\arcsin\left(\frac{m_{\rm ac}\cos(\phi)}{2}\right)-\phi\right) \end{aligned} \tag{A2}$$

From [23], the conduction loss of all semiconductor devices in the proposed topology can be represented in (A3).

Equation (A3) shows the relationship of how the duty cycle and current influence the loss of the devices. The duty decides how long the device is on, therefore, current can flow through the device to produce a conduction loss. For a device always in on-state, the conduction loss only depends on the current. For example, when the current is positive, which means the current is in the same direction with the reference current, it must flow through Q_1 or Q_4. Since Q_1 and Q_4 are always on, the conduction loss on them can be represented without duty cycle.

For other topologies listed in this paper, there are no thyristor conduction losses, but there are extra diode and IGBT losses which can be represented as (A4):

$$\begin{aligned} P_{\rm T1} &= f\cdot\int_{t_1}^{t_2}(-i(t))\cdot v_{\rm IGBT}(-i(t))d(t){\rm d}t\\ P_{\rm D1} &= f\cdot\int_{t_2-\frac{1}{f}}^{t_1} i(t)\cdot v_{\rm diode}(i(t))d(t){\rm d}t\\ P_{\rm T2} &= f\cdot\int_{t_2-\frac{1}{f}}^{t_1} i(t)\cdot v_{\rm IGBT}(i(t))(1-d(t)){\rm d}t\\ P_{\rm D2} &= f\cdot\int_{t_1}^{t_2}(-i(t))\cdot v_{\rm diode}(-i(t))(1-d(t)){\rm d}t\\ P_{\rm Q1\&Q4} &= f\cdot\int_{t_2-\frac{1}{f}}^{t_1} i(t)\cdot v_{\rm thyristor}(i(t)){\rm d}t\\ P_{\rm Q2\&Q3} &= f\cdot\int_{t_1}^{t_2}(-i(t))\cdot v_{\rm thyristor}(-i(t)){\rm d}t \end{aligned} \tag{A3}$$

$$\begin{aligned} P_{\rm extra\_diode} &= f\cdot\int_{t_2-\frac{1}{f}}^{t_1} i(t)\cdot v_{\rm diode}(i(t)){\rm d}t\\ P_{\rm extra\_IGBT} &= f\cdot\int_{t_1}^{t_2}(-i(t))\cdot v_{\rm IGBT}(-i(t)){\rm d}t \end{aligned} \tag{A4}$$

After figuring out all devices conduction loss, the total conduction loss of all existing topologies can be represented as:

$$\begin{aligned} P_{\rm HBSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ P_{\rm CDSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + P_{\rm extra\_diode}+P_{\rm extra\_IGBT}\\ P_{\rm FBSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + 2\times(P_{\rm extra\_diode}+P_{\rm extra\_IGBT})\\ P_{\rm CCDSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + 2\times(P_{\rm extra\_diode}+P_{\rm extra\_IGBT})\\ P_{\rm Mixed-cellSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + P_{\rm extra\_diode}+P_{\rm extra\_IGBT}\\ P_{\rm UFBSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + 2\times(P_{\rm extra\_diode}+P_{\rm extra\_IGBT})\\ P_{\rm CCSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + 2\times(P_{\rm extra\_diode}+P_{\rm extra\_IGBT})\\ P_{\rm SCDSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + 2\times(P_{\rm extra\_diode}+P_{\rm extra\_IGBT})\\ P_{\rm thyristor\text{-}insertedSM} &= 2\times(P_{\rm T1}+P_{\rm D1}+P_{\rm T2}+P_{\rm D2})\\ &\quad + P_{\rm Q1\&Q4}+P_{\rm Q2\&Q3} \end{aligned} \tag{A5}$$

In the specific situation where $m_{\rm ac}=0.816$, $\cos(\phi)=1$ and $I_{\rm dc}=800$, conduction loss can get a numerical solution. After that, all conduction loss can be normalized by $P_{\rm HBSM}$ to obtain normalized conduction loss in Table III.

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