Coordinated Control of Parallel Three-phase Four-wire Converters in Autonomous AC Microgrids

Rui Liu, Li Guo, *Member*, *IEEE*, and Xialin Li, *Member*, *IEEE*

***Abstract*—The coordinated control of parallel three-phase four-wire converters in autonomous AC microgrids is investigated in this paper. First, based on droop control, virtual impedance is inserted in positive-, negative- and zero-sequences to enhance system damping and imbalance power sharing. Then, to facilitate virtual impedance design, small signal models of the three-sequence equivalent circuits are established respectively. Corresponding indexes are proposed to comprehensively evaluate the impact of sequence virtual impedance on current sharing accuracy, voltage quality at the point of common coupling (PCC) and system stability. In addition, constraint of DC-link voltage is also considered to avoid over modulation when subjected to unbalanced loads. Furthermore, to address the PCC voltage degradation resulting from virtual impedance, a voltage imbalance compensation method, based on low-bandwidth communication, is proposed. Finally, simulation and experimental results are provided to verify the correctness of the theory model, indicating that the proposed method can achieve PCC voltage restoration while guaranteeing the current sharing accuracy with desirable dynamics.**

***Index Terms*—AC microgrids, sequence virtual impedance, three-phase four-wire (3P4W) converter, voltage imbalance compensation.**

NOMENCLATURE

PCC	Point of common coupling.
ESS	Energy storage system.
MG	Microgrid.
3P3W	Three-phase three-wire.
3P4W	Three-phase four-wire.
PS, NS, ZS	Positive-, negative, and zero-sequence.
LBC	Low-bandwidth communication.
MGCC	Microgrid central controller.
Conv_1, Conv_2	Converter unit 1 and 2.
SOGI-QSG	Second-order generalized integral quadrature signal generator.
PNSC	Positive/negative-sequence calculation.
SPWM	Sinusoidal pulse width modulation.
CAN	Controller area network.
PLL	Phase-locked loop.
Z_{load}	PCC load.
L_1, L_2, C, R_{d}	Parameters of the LCL filter.
L_n	Zero-sequence inductance.
Z_{line1}, Z_{line2}	Feeder impedance.
C_{dc1}, C_{dc2}	DC-link capacitors.
p, q	Instantaneous positive-sequence active and reactive power.
$u_{C\_\alpha\beta0}$	Voltage of C.
$i_{L2\_\alpha\beta0}$	Current of L_2
$i^{+}_{L2\_\alpha\beta}$	Positive-sequence current of L_2.
$i^{-}_{L2\_\alpha\beta}$	Negative-sequence current of L_2.
i_{L2_0}	Zero-sequence current of L_2.
P, Q	Filtered active and reactive power.
ω, U	Angular frequency and amplitude of the output voltage reference.
ω^*, U^*	Angular frequency and voltage amplitude references of the microgrid.
k_{Pf}, k_{QU}	Pf and QU droop gains.
P^*, Q^*	Positive-sequence active and reactive power references.
θ	Phase angle of the output voltage reference
$u_{\alpha\beta\_\text{ref}}$	Output voltage reference (without virtual impedance insertion)
$u'_{\alpha\beta0\_\text{ref}}$	Output voltage reference (with virtual impedance insertion)
L^{+}_{v}, R^{+}_{v}	Positive-sequence virtual inductance and resistance.
L^{-}_{v}, R^{-}_{v}	Negative-sequence virtual inductance and resistance.
$R_{\text{v\_0}}$	Zero-sequence virtual resistance.
$k_{\text{p\_}v}$, $k_{\text{r\_}v}$, ω_{c}	Proportional, resonant coefficient and cut-off frequency of the outer voltage loop control.
$k_{\text{i\_}v}$	Integral coefficient of the zero-sequence voltage control.
$k_{\text{p\_}i}$	Proportional coefficient of the inner current loop control.
$e_{\alpha\beta0}$	Modulation signals.
$u_{\text{com\_}\alpha\beta0}$	Voltage compensation signals.
P_i	Active power supplied by converter i.
Q_i	Reactive power supplied by converter i.
Q_{load}	Reactive power consumed by load.
U_{PCC}	Amplitude of PCC voltage.

Manuscript received July 31, 2020; revised December 31, 2020; accepted February 22, 2021. Date of online publication December 30, 2021; date of current version October 24, 2023.

R. Liu, L. Guo and X. L. Li (corresponding author, email: xialinlee@tju.edu.cn) are with the Key Laboratory of Smart Grid of Ministry of Education, Tianjin University, Tianjin 300072, China.

DOI: 10.17775/CSEEJPES.2020.03650

$u^{-}_{i\_\mathrm{com}\_\alpha\beta}$	Negative-sequence voltage compensation signals of converter i.
$u_{i\_\mathrm{com}\_0}$	Zero-sequence voltage compensation signals of converter i.
u_{dc1}, u_{dc2}, u_{dc}	Voltage of upper DC-link capacitor, lower DC-link capacitor and total DC-link bus
$\dot{I}_{\mathrm{a}}$, $\dot{I}^{+}$, $\dot{I}^{-}$, $\dot{I}_0$	Phasors of phase-A current, positive-sequence current, negative-sequence current, zero-sequence current
$\dot{U}$	Phasors of voltage reference generated by droop control.
I_n	Rated current amplitude.
ω_{PCC}, θ_{PCC}	Angular frequency and phase angle of PCC voltage.
T_{LPF}	Time constant of the low-pass filter G_{LPF}.
T_{CAN}	Communication cycle.
$k_{\mathrm{p\_com}}$, $k_{\mathrm{i\_com}}$	Proportional and integral coefficient of G_{com}.
I^{-}_{i}	Amplitude of NS currents of converter i.
I_{i_0}	Amplitude of ZS currents of converter i.

I. Introduction

ENERGY storage systems (ESSs) have been commonly used to smooth transient power fluctuations and enhance system stability in power distribution and microgrids (MGs) with large-scale integration of renewable generations [1], [2], as well as to provide auxiliary services in improving power quality and demand response [3]. Especially, in low-voltage autonomous AC MGs, ESSs play a key role in stabilizing frequency and voltage [4], [5]. Moreover, distributed ESSs, with modular parallel four-wire converters, can accommodate unbalanced loads, such as single-phase loads, without extra Y-delta transformers, as well as improve redundancy and reliability, and achieve flexible configuration with respect to different power rating considerations. Common three-phase four-wire (3P4W) converter structures can be classified as two-level three-leg [6], two-level four-leg [7], [8], three-level three-leg [9] and three-level four-leg [10], etc. Because of the advantages of low common mode voltage and low switching loss, this paper selects the T-type three-level three-leg four-wire converter. When subjected to unbalanced loads, how to enhance current sharing, improve PCC voltage quality, and ensure system stability in parallel 3P4W converters have become prominent challenges to be addressed, and are the main motivation of this paper.

To facilitate power sharing among converters in autonomous MGs when feeder impedance is mismatched, modified methods based on P-f and Q-V droop control had been developed in both three-phase three-wire (3P3W) [11]–[18] and three-phase four-wire (3P4W) [19]–[21] systems. In 3P3W systems, one practical method was to reshape the converters' output impedance by a relatively large virtual impedance, so that the discrepancy of feeder impedance could be trivialized [12], [13]. The other methods were to dynamically adjust each converter's virtual impedance in accordance with the feedbacked current information [15]–[18]. In the 3P4W system, where additional zero-sequence (ZS) current return paths existed, the design of ZS virtual impedance has been described in [19]. An intriguing method to transform power sharing issues among 3P4W converters into each phase respectively was proposed in [20], with secondary control used to eliminate deviations of the frequency, phase angle and voltage amplitude among the three phases. Nevertheless, low-bandwidths for decoupling multiple control loops may result in slow dynamics. Conservative power theory was adopted in [21] to extract balance, unbalance and harmonic current for virtual impedance applications in the a-b-c reference frame.

In the above studies, it was validated that sequence virtual impedances which far exceed the feeder impedance could help to share reactive and imbalance powers proportionally without additional communication. Although the PS and NS current sharing in 3P3W MGs have been discussed, in 3P4W MGs where an additional zero-sequence (ZS) current return path existed, ZS virtual impedance should be specially designed to realize ZS current sharing. Existing research separately investigates the design of virtual impedance for specific purposes. How to evaluate the impact of the sequence virtual impedance comprehensively and quantitatively on current sharing accuracy, PCC voltage quality and system stability is still an open area and should be clarified. In addition, voltages in light-load phases may be overmodulated if excessive negative-sequence (NS) or ZS virtual impedance is applied. DC-link voltage restriction was rarely considered in virtual impedance architecture in existing parallel 3P4W converters.

Feeder impedance, NS and ZS virtual impedance will aggravate the PCC voltage imbalance as unbalanced loads are supplied. For voltage amplitude and imbalance compensation in 3P3W systems, one approach is to change the injection of positive-sequence (PS) reactive and NS power [22]. The other is to simultaneously adjust the PS and NS voltage references of the converters according to signals generated by a centralized voltage compensator [23]–[25]. A distributed voltage recovery method, through exchanging the integral items of the secondary controllers, is proposed in [26] to achieve voltage compensation and power sharing at the same time, but the scenario in which mismatched feeder impedance occurs hasn't been considered. In the 3P4W system, the extra ZS component in PCC voltage should be taken into consideration. Existing key-node voltage imbalance compensation methods by means of virtual impedance adaptation [19] tend to decrease current sharing accuracy. Using the signal transformation contrived in [23]–[25] to translate ZS voltage signals into DC quantities for transmission by low-bandwidth communication (LBC) seems to be a feasible solution for ZS voltage compensation. Therefore, how to compensate the imbalance of PCC voltage in 3P4W MGs while maintaining the current sharing accuracy requires further study.

The main motivation of this paper is to address the aforementioned issues of parallel 3P4W converters in islanded AC MGs. First, the DC-link voltage restriction for virtual impedance design is formulated to avoid over modulation. Second, corresponding indexes are comprehensively and quantitatively proposed to evaluate the impact of sequence virtual impedance on current sharing accuracy, PCC voltage quality and system stability, so as to achieve the optimal and robust design of virtual impedance. Third, a voltage imbalance com-

pensation method based on LBC is proposed to realize voltage compensation. Compared with methods for 3P3W MGs [23]–[25], compensators for mitigating ZS components of PCC voltage in 3P4W AC MGs are elaborately designed to provide high quality power for single-phase loads. Meanwhile, the accuracy of current sharing is ensured.

The remainder of this paper is organized as follows. The structure of parallel 3P4W converters is illustrated in Section II. In Section III, basic P-f and Q-V droop with sequence virtual impedance for parallel 3P4W converters is first reviewed. Then, small signal models of the three sequence circuits are established. Moreover, corresponding indexes are quantitatively proposed to evaluate the impact of sequence virtual impedance on the 3P4W system. In Section IV, the voltage imbalance compensation method based on LBC is presented. Simulation and experimental validations are provided in Sections V and VI respectively. Section VII concludes this paper.

II. Configuration of AC MG Composed of Parallel 3P4W Converters

The considered 3P4W AC MG is illustrated in Fig. 1. Two converter units (Conv_1 and Conv_2) and PCC loads (Z_{load}) are connected to the common AC bus. Each converter is controlled by a local controller in real time, which is connected to the microgrid central controller (MGCC) via LBC. Algorithms embedded in the local controller achieve voltage control and power sharing according to P-f and Q-V droop characteristics. The MGCC samples and processes the PCC voltage to generate PS, NS and ZS voltage compensation signals, which are broadcasted to converter units to realize voltage imbalance compensation. The LCL structure is employed as an AC side filter, whose neutral point is connected to that of the DC link capacitors via L_n [27]. $Z_{\text{line\_1}}$ and $Z_{\text{line\_2}}$ represent the discrepancies between the feeder lengths and series reactors for refining the harmonic characteristics of specific converters. C_{dc1} and C_{dc2} can be directly connected to batteries or through a front-end DC/DC interface. To simplify the discussion, ideal DC-link capacitors with constant DC voltage are assumed in this paper [14].

III. Impact of Sequence Virtual Impedance on Current Sharing, PCC Voltage Quality and System Stability

A. Implementation of Local Controller

As shown in Fig. 1, the local controller consists of a power calculation, droop control, current extraction, virtual impedance and voltage control.

1) Power Calculation: p and q are calculated according to $u_{C\_\alpha\beta0}$ and $i^{+}_{L2\_\alpha\beta}$ in (1). Then, p and q are filtered by low-pass filters, yielding P and Q respectively.

$$\begin{cases} p = 1.5\left(u_{C\_\alpha} i^{+}_{L2\_\alpha} + u_{C\_\beta} i^{+}_{L2\_\beta}\right) \\ q = 1.5\left(u_{C\_\beta} i^{+}_{L2\_\alpha} - u_{C\_\alpha} i^{+}_{L2\_\beta}\right) \end{cases} \tag{1}$$

2) Droop Control: P-f and Q-V droop control is implemented by (2):

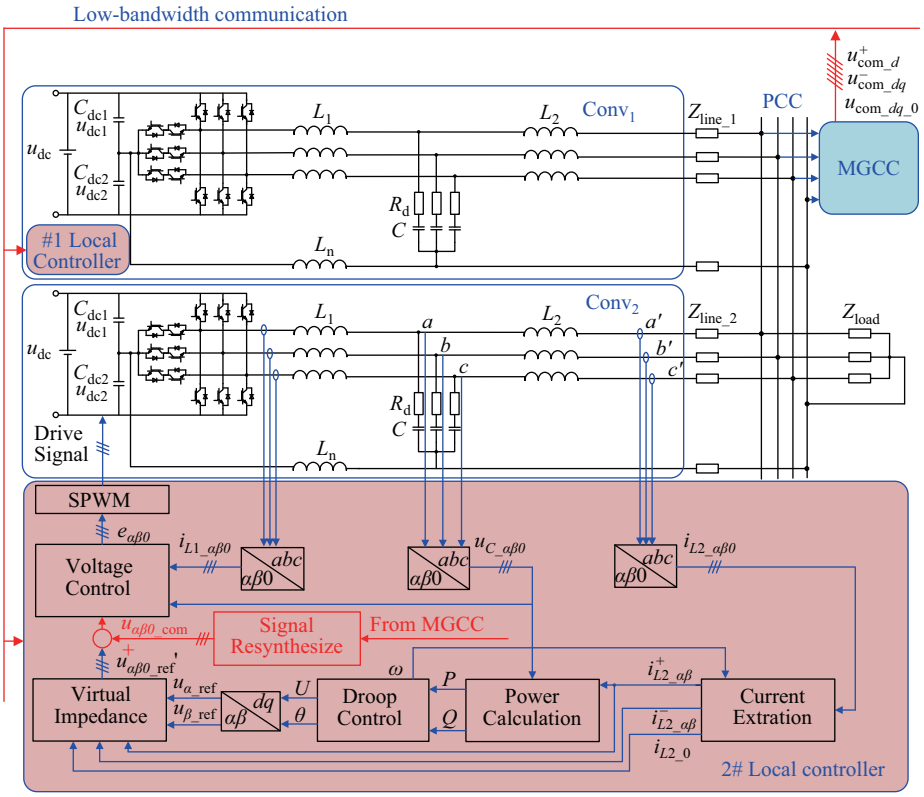


Fig. 1. Schematic of 3P4W AC MG.

$$\begin{cases} \omega = \omega^* + k_{Pf}(P^* - P) \\ U = U^* + k_{QU}(Q^* - Q) \end{cases} \tag{2}$$

where θ can be derived by the integration of ω.

3) Current Extraction and Virtual Impedance: A Second-order generalized integral quadrature signal generator (SOGI-QSG) and positive-/negative-sequence calculation (PNSC) [28] are utilized to extract fundamental currents $i^+_{L2\_\alpha\beta}$, $i^-_{L2\_\alpha\beta}$ and i_{L2_0}. In order to share the currents and enhance system stability, when feeder impedance mismatch occurs, the sequence virtual impedance is generally inserted as (3):

$$\begin{cases} u'_{\alpha\_\text{ref}} = u_{\alpha\_\text{ref}} - R^+_\text{v} i^+_{L2\_\alpha} + \omega L^+_\text{v} i^+_{L2\_\beta} \\ \qquad\qquad - R^-_\text{v} i^-_{L2\_\alpha} - \omega L^-_\text{v} i^-_{L2\_\beta} \\ u'_{\beta\_\text{ref}} = u_{\beta\_\text{ref}} - \omega L^+_\text{v} i^+_{L2\_\alpha} - R^+_\text{v} i^+_{L2\_\beta} \\ \qquad\qquad + \omega L^-_\text{v} i^-_{L2\_\alpha} - R^-_\text{v} i^-_{L2\_\beta} \\ u'_{0\_\text{ref}} = -R_{\text{v}0} i_{L2\_0} \end{cases} \tag{3}$$

where $u_{\alpha\beta\_\text{ref}}$ are generated by $dq/\alpha\beta$ transformation of U and θ. $u'_{\alpha\beta0\_\text{ref}}$ can be acquired after adding the sequence virtual impedance.

4) Voltage Control: In the voltage control loop, quasi-proportional resonant control (G_{v_PR}) is adopted for the voltage outer loop. An extra integral item is employed in the ZS voltage control (G_{v_PIR}) to eliminate the DC component. Proportional control (G_i) is utilized for the current inner loop. $e_{\alpha\beta0}$ is modulated by sinusoidal pulse width modulation (SPWM) to generate a driving signal for the semiconductor devices. When the voltage compensation is enabled, signals from the MGCC are resynthesized into the $\alpha\beta0$ reference frame and added to $u'_{\alpha\beta0\_\text{ref}}$ as shown in the red part of Fig. 1.

$$\begin{cases} G_{v\_\text{PR}} = k_{\text{p}\_v} + \frac{2k_{\text{r}\_v}\omega_\text{c} s}{s^2+2\omega_\text{c} s+\omega^2} \\ G_{v\_\text{PIR}} = k_{\text{p}\_v} + \frac{k_{\text{i}\_v}}{s} + \frac{2k_{\text{r}\_v}\omega_\text{c} s}{s^2+2\omega_\text{c} s+\omega^2} \\ G_i = k_{\text{p}\_i} \end{cases} \tag{4}$$

It is noteworthy that the model here is used for refining the primary-level control, so $u_{\text{com}\_\alpha\beta0}$ is regarded as a constant with the dynamics of the secondary-level control omitted. Using an AC MG composed of two parallel 3P4W converters as an example, according to the theorem of symmetrical components, small-signal models of the three-sequence circuits can be established respectively [19].

B. Impact of PS Virtual Impedance on Reactive Power Sharing, PCC Voltage Amplitude and System Stability

In the PS circuit, the modeling method based on the complex number matrix is adopted [13]. Around the equilibrium point, (5) can be derived by introducing a small disturbance $[\Delta\theta_1, \Delta\theta_2, \Delta U_{C\_1}, \Delta U_{C\_2}]^\text{T}$ to the voltage reference angles and amplitudes of Conv_1 and Conv_2 which is illustrated in appendix A. Apparently, the characteristic equation of the PS circuit is $\det(\boldsymbol{G}^+) = 0$.

$$\begin{aligned} &\boldsymbol{G}^+\boldsymbol{X} = 0 \\ &\boldsymbol{X} = [\Delta\theta_1 \quad \Delta\theta_2 \quad \Delta U_{C\_1} \quad \Delta U_{C\_2}]^\text{T} \end{aligned} \tag{5}$$

According to the parameters of a mainstream modular 3P4W converter in Table I, stability of the PS circuit is discussed. As shown in Fig. 2, with the increase of the PS virtual inductance value, dominant conjugate poles Eig.1 and Eig.2 approach the real axis with the damping ratio ζ^+ increasing. Then Eig.1 and Eig.2 convert to negative real poles and the system is overdamped. However, when PS virtual inductance further increases, one of the negative real poles goes to the origin, which indicates that the system becomes less stable.

TABLE I
PARAMETERS OF THE 3P4W CONVERTER

Sub System	Parameter	Variable	Value
Power stage	Rated power	S_rated	30 kVA
	LCL filter	L_1, C	500 μH, 20 μF
		(R_d), L_2	(0.22 Ω), 120 μH
	Zero-sequence inductance	L_n	500 μH
	DC-link capacitors voltage	$u_{\text{dc}1}$, $u_{\text{dc}2}$	350 V, 350 V
Control system	Power time constant	T_{PQ_LPF}	0.0017 s
	Rated angular frequency	ω^*	314 rad/s
	Rated voltage amplitude	U^*	311 V
	Pf droop gain	k_{Pf}	0.10472 kW/(rad/s)
	QU droop gain	k_{QU}	0.33 kVar/V
	Voltage control	k_{p_v}, k_{i_v}, ω_c	1, 10, 6.5 rad/s
	Current control	k_{p_i}	0.8
	Switching frequency	T_s	15 kHz

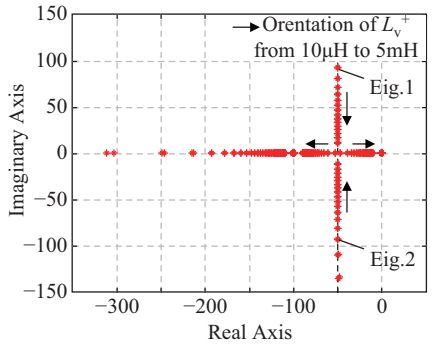


Fig. 2. Closed-loop poles of PS circuit.

To evaluate the accuracy of PS reactive power sharing, PS unit circulating reactive power λ^+_Q is defined in (6). The rate of voltage amplitude deviation λ^+_u can be defined as (7).

$$\lambda^+_Q = \frac{|Q_1 - Q_2|}{Q_\text{load}} \times 100\% \tag{6}$$

$$\lambda^+_u = \frac{|U_\text{PCC} - U^*|}{U^*} \times 100\% \tag{7}$$

Let the feeder impedance of Conv_1 and Conv_2 be 100 μH + 0.01 Ω and 200 μH + 0.02 Ω respectively. To ensure power decoupling, only virtual inductance is employed. ζ^+, λ^+_Q and λ^+_u with the variation of L^+_v are shown in Fig. 3. With the increase of the PS virtual inductance, the PS unit circulating reactive power decreases and the stability of the PS circuit increases, and the PCC voltage amplitude deviation increases.

C. Impact of NS Virtual Impedance on NS Current Sharing, NS Component in PCC Voltage and System Stability

When the PS circuit is stable, ω stays constant and $u_{\alpha\beta\_\text{ref}}$ generated by the droop control contains only the PS component. The NS current consumed by unbalanced loads can

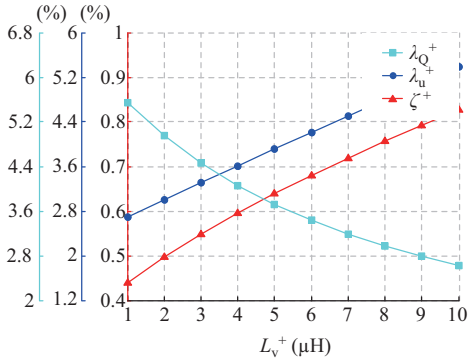


Fig. 3. Relationship between L_v^+ and ζ^+, λ_Q^+, λ_u^+.

be modeled as a current source $i_{L2\_\alpha\beta}^-$ [14]. According to the superposition theorem, it is assumed that $i_{L2\_\alpha\beta0}$ contains only NS component $i_{L2\_\alpha\beta}^-$. The transfer function of the NS circuit is formulated in (8) and the detail expression of $\boldsymbol{G}_1^-$, $\boldsymbol{G}_2^-$ and $\boldsymbol{Z}^-$ can be found in Appendix B.

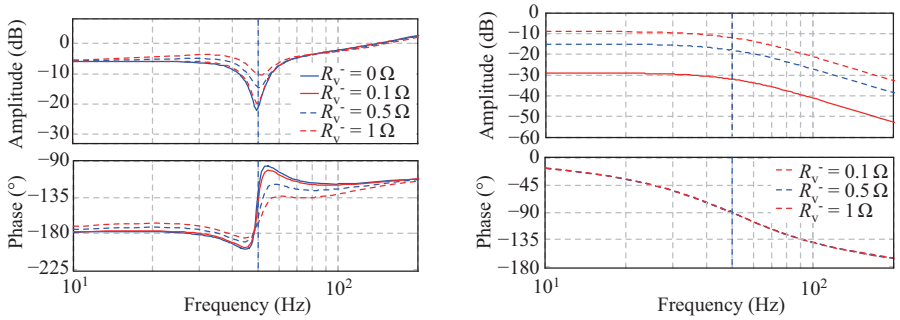
$$\begin{bmatrix} u_{\mathrm{PCC\_}\alpha}^- \\ u_{\mathrm{PCC\_}\beta}^- \end{bmatrix} = \boldsymbol{G}_1^- \begin{bmatrix} u_{1\_\mathrm{com\_}\alpha}^- \\ u_{1\_\mathrm{com\_}\beta}^- \end{bmatrix} + \boldsymbol{G}_2^- \begin{bmatrix} u_{2\_\mathrm{com\_}\alpha}^- \\ u_{2\_\mathrm{com\_}\beta}^- \end{bmatrix} + \boldsymbol{Z}^- \begin{bmatrix} i_{L2\_\alpha}^- \\ i_{L2\_\beta}^- \end{bmatrix} \tag{8}$$

For a typical case that only NS virtual resistance R_v^- is inserted, the Bode diagrams of elements in NS equivalent impedance matrix $\boldsymbol{Z}^-$ are shown in Fig. 4. The amplitude-frequency and phase-frequency characteristics of diagonal elements in $\boldsymbol{Z}^-$ (i.e., α-α axis and β-β axis impedance) are consistent, and the amplitude-frequency response around the fundamental frequency increases with R_v^-. The phase-frequency characteristics of off-diagonal elements (i.e., α-β axis and β-α axis impedance) differ by 180 ° and the amplitude-frequency response around the fundamental frequency increases with R_v^-. Therefore, the NS equivalent impedance around the fundamental frequency can be controlled by R_v^-. The Bode diagrams of the elements in the NS voltage control matrix $\boldsymbol{G}_1^-$ are shown in Fig. 5. Considering that NS current is concentrated around the fundamental frequency and the component α lags the component β by 90°, through extracting the characteristics of each element in $\boldsymbol{G}_1^-$, $\boldsymbol{G}_2^-$, and $\boldsymbol{Z}^-$ around fundamental frequency, (8) can be simplified as (9). It is obvious that the equivalent impedance of the NS circuit is dominated by the NS virtual resistance.

$$\begin{aligned} \begin{bmatrix} u_{\mathrm{PCC\_}\alpha}^- \\ u_{\mathrm{PCC\_}\beta}^- \end{bmatrix} \approx & \begin{bmatrix} 1/2 & 0 \\ 0 & 1/2 \end{bmatrix} \begin{bmatrix} u_{1\_\mathrm{com\_}\alpha}^- \\ u_{1\_\mathrm{com\_}\beta}^- \end{bmatrix} \\ & + \begin{bmatrix} 1/2 & 0 \\ 0 & 1/2 \end{bmatrix} \begin{bmatrix} u_{2\_\mathrm{com\_}\alpha}^- \\ u_{2\_\mathrm{com\_}\beta}^- \end{bmatrix} - \frac{R_v^-}{2} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L2\_\alpha}^- \\ i_{L2\_\beta}^- \end{bmatrix} \end{aligned} \tag{9}$$

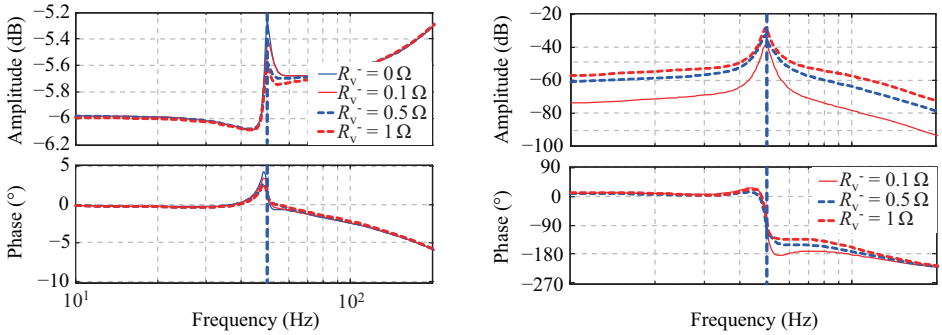
Closed-loop poles of the NS circuit are shown in Fig. 6. As the NS virtual resistance increases, dominant conjugate poles Eig.1 and Eig.2 show an inconspicuous trend of approaching the imaginary axis, indicating that the impact on system stability is trivial.

In order to evaluate the error of NS current sharing, NS unit circulating current λ_i^- is defined as (10). PCC NS voltage λ_u^- resulted from unit NS current can be defined as (11).



(a) $\boldsymbol{Z}_1^-$ (1, 1) (b) $\boldsymbol{Z}_1^-$ (2, 1)

Fig. 4. Bode diagram of main elements in $\boldsymbol{Z}^-$.



(a) $\boldsymbol{G}_1^-$ (1, 1) (b) $\boldsymbol{G}_1^-$ (2, 1)

Fig. 5. Bode diagram of main elements in $\boldsymbol{G}_1^-$.

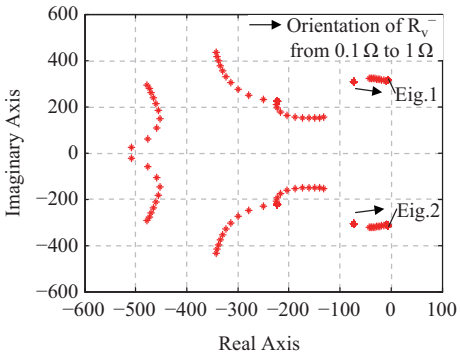


Fig. 6. Closed-loop poles of negative-sequence circuit.

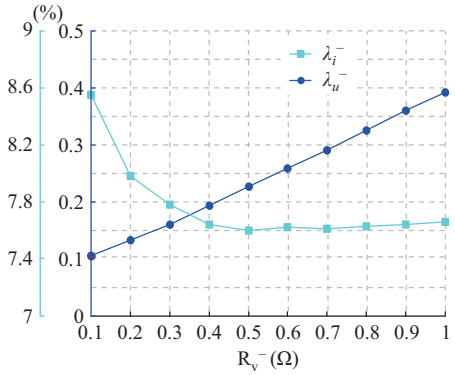


Fig. 7. Relationship between R_v^- and λ_i^-, λ_u^-.

λ_i^- and λ_u^- with the variation of R_v^- are shown in Fig. 7. With the increase of the NS virtual resistance, the NS current sharing error decreases, but the NS component in PCC voltage increases.

$$\begin{cases} \begin{bmatrix} \Delta i_{L2\_\alpha}^- \\ \Delta i_{L2\_\beta}^- \end{bmatrix} = \begin{bmatrix} i_{L2\_1\_\alpha}^- \\ i_{L2\_1\_\beta}^- \end{bmatrix} - \begin{bmatrix} i_{L2\_2\_\alpha}^- \\ i_{L2\_2\_\beta}^- \end{bmatrix} = \boldsymbol{G}_{\Delta i}^- \begin{bmatrix} i_{L2\_\alpha}^- \\ i_{L2\_\beta}^- \end{bmatrix} \\ \lambda_i^- = \sqrt{\dfrac{\Delta {i_{L2\_\alpha}^-}^2 + \Delta {i_{L2\_\beta}^-}^2}{{i_{L2\_\alpha}^-}^2 + {i_{L2\_\beta}^-}^2}}\Bigg|_{\omega=\omega*} \times 100\% \end{cases} \tag{10}$$

$$\lambda_u^- = \sqrt{\frac{{u_{\mathrm{PCC\_}\alpha}^-}^2 + {u_{\mathrm{PCC\_}\beta}^-}^2}{{i_{L2\_\alpha}^-}^2 + {i_{L2\_\beta}^-}^2}}\Bigg|_{\omega=\omega*} \tag{11}$$

D. Impact of ZS Virtual Impedance on ZS Current Sharing, ZS Component in PCC Voltage and System Stability

The ZS current consumed by unbalanced loads can be modeled as a current source i_{L2_0} [19]. According to the superposition theorem, it is assumed that the $i_{L2\_\alpha\beta0}$ contains only ZS component i_{L2_0}. The transfer function of the ZS circuit is formulated in (12) and the detail expression of G_{0_1}, G_{0_2} and Z_0 can be found in Appendix D.

$$u_{\mathrm{PCC\_0}} = G_{0\_1} u_{1\_\mathrm{com\_0}} + G_{0\_2} u_{2\_\mathrm{com\_0}} + Z_0 i_{L2\_0} \tag{12}$$

For a typical case that only virtual resistance $R_{\mathrm{v\_0}}$ is inserted, the Bode diagram of system ZS equivalent impedance Z_0 is shown in Fig. 8(a). The ZS equivalent impedance around the fundamental frequency can be controlled by $R_{\mathrm{v\_0}}$. The Bode diagrams of ZS voltage control transfer function G_{0_1} is shown in Fig. 8(b). Considering that ZS current is concentrated around the fundamental frequency, by extracting the characteristics of G_{0_1}, G_{0_2}, and Z_0 around fundamental frequency, (12) can be simplified as (13). It is obvious that the equivalent impedance of the ZS circuit is dominated by the ZS virtual resistance.

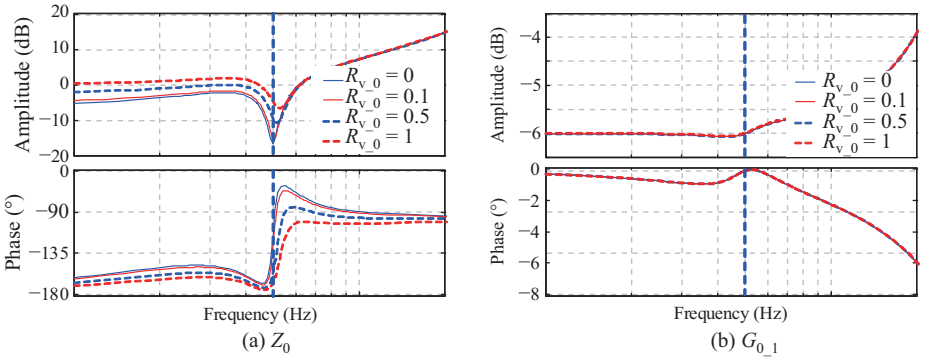
$$u_{\mathrm{PCC\_0}} = \frac{1}{2} u_{1\_\mathrm{com\_0}} + \frac{1}{2} u_{2\_\mathrm{com\_0}} - \frac{R_{\mathrm{v\_0}}}{2} i_{L2\_0} \tag{13}$$

Closed-loop poles of the ZS circuit are shown in Fig. 9. As the increase of ZS virtual resistance, conjugate poles Eig.1 and Eig.2 approach the imaginary axis. Conjugate poles Eig.3 and Eig.4 move away from the imaginary axis. Overall, the system stability is generally unchanged with the variation of ZS virtual.

In order to evaluate the error of ZS current sharing, ZS unit circulating current λ_{i_0} is defined in (14). PCC ZS voltage λ_{u_0} resulted from unit ZS current can be defined as (15). λ_{i_0} and λ_{u_0} with the variation of $R_{\mathrm{v\_0}}$ are shown in Fig. 10. With the increase of the ZS virtual resistance, the ZS current sharing error decreases, but the ZS component in PCC voltage increases.

$$\begin{cases} \Delta i_{L2\_0} = i_{L2\_1\_0} - i_{L2\_2\_0} = G_{\Delta i\_0} i_{L2\_0} \\ \lambda_{i\_0} = \dfrac{\Delta i_{L2\_0}}{i_{L2\_0}}\Bigg|_{\omega=\omega*} \times 100\% \end{cases} \tag{14}$$

$$\lambda_{u\_0} = \frac{u_{\mathrm{PCC\_0}}}{i_{L2\_0}}\Bigg|_{\omega=\omega*} \tag{15}$$



(a) Z_0 (b) G_{0_1}

Fig. 8. Bode diagrams of Z_0 and G_{0_1}.

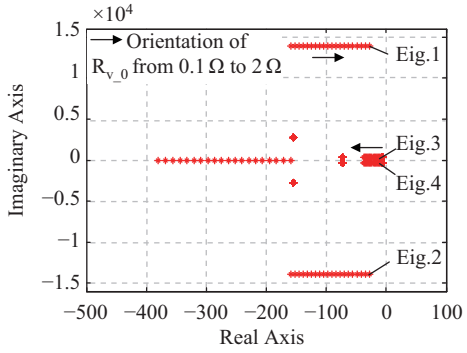


Fig. 9. Closed-loop poles of zero-sequence circuit.

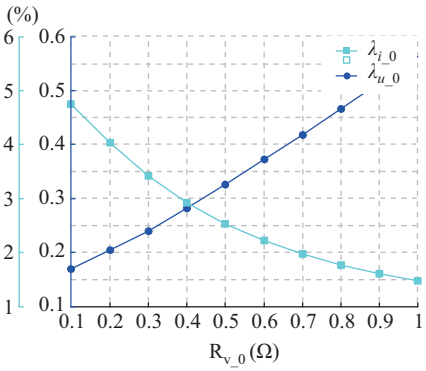


Fig. 10. Relationship between $R_{\mathrm{v\_0}}$ and λ_{i_0}, λ_{u_0}.

E. Constraint of the DC-Link Voltage

When unbalanced loads are supplied, voltages in the phase with light loads are prone to over modulate if excessive NS or ZS virtual impedance is inserted. Half of the DC-link voltage should be higher than the total voltage drops on the filter capacitor, the filter inductor and the neutral inductor in each phase. Using phase A as an example, the constraint can be prescribed as:

$$\frac{u_{\mathrm{dc}}}{2} \geq |j\omega L_1 \dot{I}_{\mathrm{a}} + j\omega L_{\mathrm{v}}^{+}\dot{I}^{+} + R_{\mathrm{v}}^{-}\dot{I}^{-} + (R_{\mathrm{v\_0}} + j\omega L_n)\dot{I}_0 + \dot{U}| \tag{16}$$

For a general case, three-phase loads with the same power factor and different amplitude are supplied. The maximum value of the amplitude of $\dot{I}_{\mathrm{a}}$, $\dot{I}^{+}$, $\dot{I}^{-}$ can be deduced as I_n, $I_n/3$ and $I_n/3$ respectively. The maximum value of the right-side expression of (16) can be derived as:

$$\begin{aligned} &|j\omega L_1 \dot{I}_{\mathrm{a}} + j\omega L_{\mathrm{v}}^{+}\dot{I}^{+} + R_{\mathrm{v}}^{-}\dot{I}^{-} + (R_{\mathrm{v\_0}} + j\omega L_n)\dot{I}_0 + \dot{U}| \leq \\ &|j\omega L_1 \dot{I}_{\mathrm{a}}| + |j\omega L_{\mathrm{v}}^{+}\dot{I}^{+}| + |R_{\mathrm{v}}^{-}\dot{I}^{-}| + |(R_{\mathrm{v\_0}} + j\omega L_n)\dot{I}_0| + |\dot{U}| \leq \\ &I_n\left(\omega(L_1 + L_{\mathrm{v}}^{+}) + \frac{R_{\mathrm{v}}^{-} + \sqrt{R_{\mathrm{v\_0}}^2 + (\omega L_n)^2}}{3}\right) + U_{\max} \end{aligned} \tag{17}$$

where $U_{\max}$ is the maximum value of the voltage amplitude reference generated by droop control. Therefore, the constraint of DC-link voltage for designing the sequence virtual impedance is shown as:

$$\frac{u_{\mathrm{dc}}}{2} \geq I_n\left(\omega(L_1 + L_{\mathrm{v}}^{+}) + \frac{R_{\mathrm{v}}^{-} + \sqrt{R_{\mathrm{v\_0}}^2 + (\omega L_n)^2}}{3}\right) + U_{\max} \tag{18}$$

IV. Voltage Imbalance Compensation Method Based on Low-Bandwidth Communication

According to the analysis in Section III, in the 3P4W system, the insertion of three-sequence virtual impedance will cause PCC voltage degradation, including amplitude deviation and imbalance, which aggravates with the load increasing. A controller area network (CAN) has been extensively used in industrial field, and is selected as the LBC for the transmission

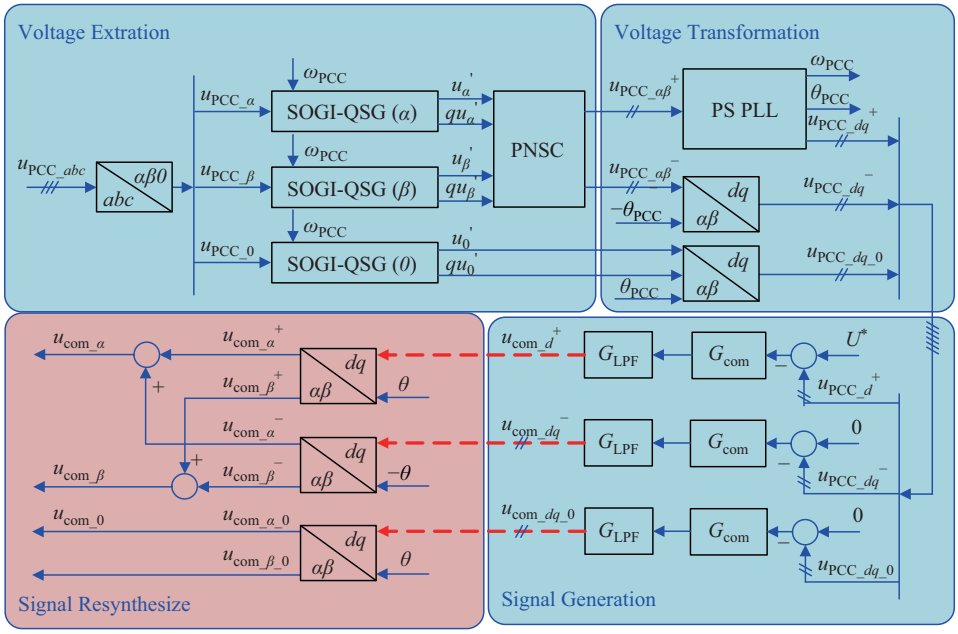


Fig. 11. Schematic of the voltage imbalance compensation method.

of compensation signals in this paper. The generation of compensation signals in MGCC can be summarised as follows.

1) Step 1: As illustrated in "Voltage Extraction" in Fig. 11, PS, NS and ZS components in PCC voltage are extracted by SOGI-QSG and PNSC. In "Voltage Transformation, " the PS component is processed by phase-locked loop (PLL) to obtain ω_{PCC} and θ_{PCC}. Then, the PS and ZS components are transformed into DC quantities in the rotating reference frame indicated by θ_{PCC}. The NS component is transformed into DC quantities in the rotating reference frame indicated by $-\theta_{\mathrm{PCC}}$, which rotates in the same frequency and opposite direction compared with the PS frame.

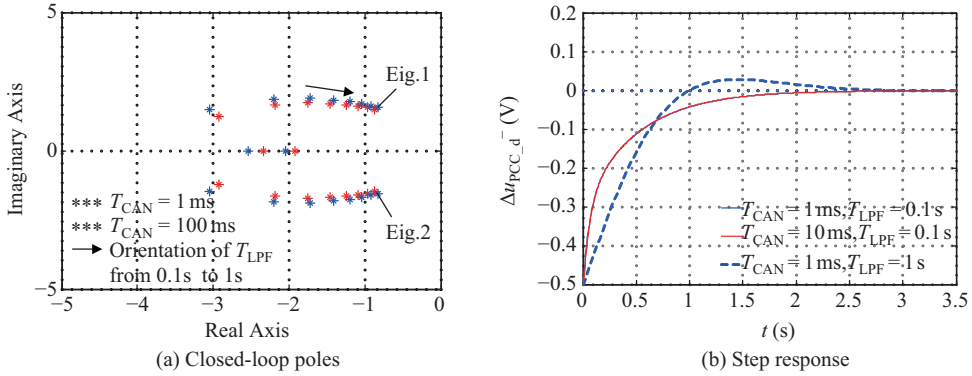
2) Step 2: As illustrated in "Signal Generation" of Fig. 11, the corresponding rotating reference frames, proportional integral control (G_{com}) and low-pass filter (G_{LPF}) are performed to generate compensation signals, which are then sent to each local controller through CAN.

The signal resynthesize embedded in the local controller is shown in "Signal Resynthesize" of Fig. 11. Due to the phase angle deviation between the voltage at point a, b, c illustrated in Fig. 1, and PCC is trivial, and $\theta \approx \theta_{\mathrm{PCC}}$ can be assumed. The received PS, NS and ZS compensation signals are inversely transformed into stationary frames. Then the three-sequence compensation signals in the stationary frame are synthesised and added to the position as shown in Fig. 1. The compensation for PCC voltage imbalance is accomplished.

Because the bandwidth of the compensation signal generation in Fig. 11 is relatively low, the dynamics of PCC voltage extraction and PLL in MGCC, and the dynamics of the voltage compensation signals conduction in local controllers can be neglected when the procedure of voltage restoration is modeled. According to Appendix D, a simplified PS, NS and ZS voltage compensation closed-loop transfer function can be derived as (19). Around the equilibrium point, small disturbances ΔY_{load}, Δi_{dq}^{-} and Δi_{dq_0}, namely, PS load disturbance, NS and ZS current disturbances are introduced. ΔU_{PCC}, $\Delta u_{\mathrm{pcc}\_dq}^{-}$ and $\Delta u_{\mathrm{pcc}\_dq\_0}$, namely, the PCC PS, NS and ZS voltage small signal variation can be obtained. G_{CAN} represents the delay resulting from CAN, which can be approximated by a second-order Pade approximation.

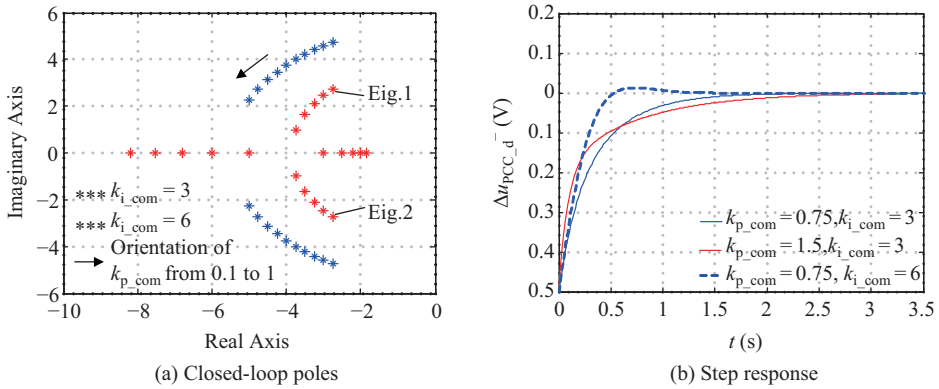
Using the NS voltage compensation closed-loop transfer function in (19) for example, in Fig. 12, as T_{LPF} increases, the closed-loop poles Eig.1 and Eig.2 approach the imaginary axis and the voltage overshoot increases, which indicates that the system stability decreases. The variation of T_{CAN} in a wide range (1 ms–100 ms) has an inconspicuous effect on the system stability dynamics, indicating that the proposed voltage compensation method has relatively low requirements for the bandwidth of communication. Considering the variables to be transmitted in a communication cycle, (extended) frame format of CAN, constraint of baud rate for different bus length and typical load rate (30%), the minimum communication cycle can be obtained in Table II.

As shown in Fig. 13(a), as $k_{\mathrm{p\_com}}$ increases from 0.1 to 1, the closed-loop poles Eig.1 and Eig.2 approach the real axis with the damping ratio increasing. Then Eig.1 and



(a) Closed-loop poles (b) Step response

Fig. 12. The impact of T_{CAN} and T_{LPF} on system stability.



(a) Closed-loop poles (b) Step response

Fig. 13. The impact of $k_{\mathrm{p\_com}}$ and $k_{\mathrm{i\_com}}$ on system stability.

TABLE II
MINIMUM COMMUNICATION CYCLE OF CAN

Baud rate (bps)	Max bus length (m)	Min communication cycle (ms)
1 M	40	0.85
500 k	130	1.7
125 k	530	6.7
50 k	1.3 k	17

Eig.2 convert to negative real poles, which shows that the system is overdamped. As $k_{\mathrm{i\_com}}$ increases from 3 to 6, the damping ratio of closed-loop poles Eig.1 and Eig.2 is reduced. As shown in Fig. 13(b), the NS voltage recovers faster at the beginning of the step response when $k_{\mathrm{p\_com}}$ switches from 0.75 to 1.5 and the recovery is accelerated with larger overshoot when $k_{\mathrm{i\_com}}$ switches from 3 to 6.

$$\begin{cases} \Delta U_{\mathrm{PCC}} = \dfrac{\partial U_{\mathrm{PCC}}/\partial Y_{\mathrm{load}}}{\left(2\dfrac{\partial U_{\mathrm{PCC}}}{\partial U_{C\_1}}G_{\mathrm{com}}G_{\mathrm{LPF}}G_{\mathrm{CAN}}+1\right)}\Delta Y_{\mathrm{load}} \\ \Delta u_{\mathrm{PCC\_}dq\_0} = \dfrac{-R_{\mathrm{v\_}0}}{2\left(G_{\mathrm{com}}G_{\mathrm{LPF}}G_{\mathrm{CAN}}+1\right)}\Delta i_{L2\_dq\_0} \\ \Delta u^{-}_{\mathrm{PCC\_}dq} = \dfrac{-R^{-}_{\mathrm{v}}}{2\left(G_{\mathrm{com}}G_{\mathrm{LPF}}G_{\mathrm{CAN}}+1\right)}\Delta i^{-}_{L2\_dq} \end{cases} \tag{19}$$

V. SIMULATION VERIFICATION

A. Simulation Platform

In order to verify the correctness of the theory model and the feasibility of the proposed PCC voltage imbalance compensation method, according to the parameters in Table I, the electromagnetic transient simulation model of a 3P4W AC MG composed of two parallel converters is established in MATLAB/Simulink. The feeder impedance of the Conv_1 and Conv_2 are 100 μH + 0.01 Ω and 200 μH + 0.02 Ω respectively. Parameters of voltage compensation control T_{CAN}, T_{LPF}, $k_{\mathrm{p\_com}}$ and $k_{\mathrm{i\_com}}$ are set at 0.001, 0.1, 0.5 and 1 respectively. To evaluate the voltage unbalance, the voltage unbalance factors (VUF^{-} and VUF^{0}, indicating the relative NS and ZS components in PCC voltage) are introduced as defined in (20) [29], where $|u^{+}_{\mathrm{PCC}}|$, $|u^{-}_{\mathrm{PCC}}|$ and $|u_{\mathrm{PCC\_0}}|$ represent the amplitudes of the PS, NS and ZS components in PCC voltage respectively.

$$\begin{cases} \mathrm{VUF}^{-} = \dfrac{|u^{-}_{\mathrm{PCC}}|}{|u^{+}_{\mathrm{PCC}}|}\cdot 100\% \\ \mathrm{VUF}^{0} = \dfrac{|u_{\mathrm{PCC\_0}}|}{|u^{+}_{\mathrm{PCC}}|}\cdot 100\% \end{cases} \tag{20}$$

B. Simulation Case 1

Relevant conclusions on the modeling for the NS and ZS circuits are verified in case 1. As shown in Fig. 14, L^{+}_{v} is set at 1 mH and the single-phase load of 16 kW in phase A is supplied. First, R^{-}_{v} and $R_{\mathrm{v\_0}}$ switch from zero to 0.5 Ω and 1 Ω respectively at 1 s. The NS current sharing error decreases from 3.2 A to 0.35 A. The ZS current sharing error decreases from 6.5 A to 0.9 A. VUF^{-} increases from 0.9%

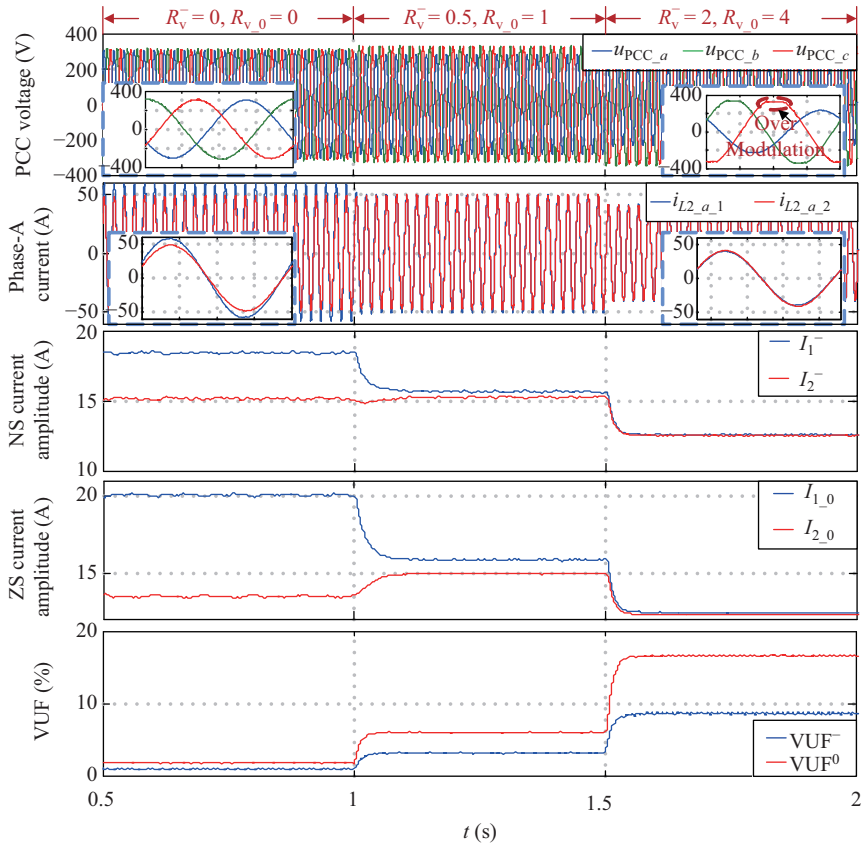


Fig. 14. Simulation results of case 1.

to 3.2% and VUF^0 increases from 1.75% to 6%. R_{v}^- and $R_{\mathrm{v\_0}}$ further increase to relatively large values of 2 Ω and 4 Ω respectively at 1.5 s. The system stays stable, and an obvious over modulation area can be noticed in the voltage of phase C. The simulation results indicate that as the NS and ZS virtual resistances increase, the NS and ZS current sharing errors decrease, but the PCC voltage imbalance increases and over modulation may occur in phases with light loads.

C. Simulation Case 2

The PCC voltage imbalance compensation method is verified in case 2. First, L_{v}^+, R_{v}^- and $R_{\mathrm{v\_0}}$ are set at 1 mH, 0.5 Ω and 1 Ω, respectively. Three-phase unbalanced loads consisting of 5 kW in phase A, 10 kW in phase B and 20 kW in phase C are supplied. The voltage compensation is enabled at 1 s. As shown in Fig. 15, before and after the voltage compensation is enabled, NS current sharing errors are 0.2 A and 0.35 A. ZS current sharing errors are 0.7 A and 0.9 A. VUF^- decreases from 2.5% to 0.5% and VUF^0 decreases from 4.5% to 0.2%. PCC three-phase voltage amplitudes change from 328/321/288 V to 315/312/310 V. The simulation results indicate that the PCC voltage compensation method can achieve the compensation of PCC voltage amplitude and imbalance, meanwhile it has almost no effect on the current sharing accuracy.

D. Simulation Case 3

The dynamics of the PCC voltage imbalance compensation method is analyzed in case 3. First, L_{v}^+, R_{v}^- and $R_{\mathrm{v\_0}}$ are set at 1 mH, 0.5 Ω and 1 Ω respectively. PCC voltage compensation is enabled. Three-phase balanced loads, consisting of 10 kW per phase, are supplied before 1 s and then the phase-A load is increased by 10 kW at 1 s. As shown in Fig. 16, VUF^- and VUF^0 recover to the steady-state value within 0.5 s after the load step, and the recovery time increases with the increase of T_{LPF}. Simulation results indicate that the desired dynamics of the proposed PCC voltage compensation method can be achieved by tuning T_{LPF} properly.

VI. Experimental Verification

A. Experimental Platform

To verify the theoretical model and voltage imbalance compensation method proposed in this paper, according to the parameters in Table I, a MG experimental platform composed of two parallel converters is established as shown in Fig. 17. The feeder impedance of the Conv_1 and Conv_2 are zero and 300 μH respectively.

B. Experimental Case 1

Relevant conclusions on the modeling for three-sequence circuits in Section III are verified in case 1. First, L_{v}^+, R_{v}^- and $R_{\mathrm{v\_0}}$ are all set at zero. Three-phase unbalanced loads, consisting of 9 kW in phase A, 3 kW in phase B and 1 kW in phase C, are supplied. The amplitudes of PCC voltages (310/314/308 V) and three-phase output currents of

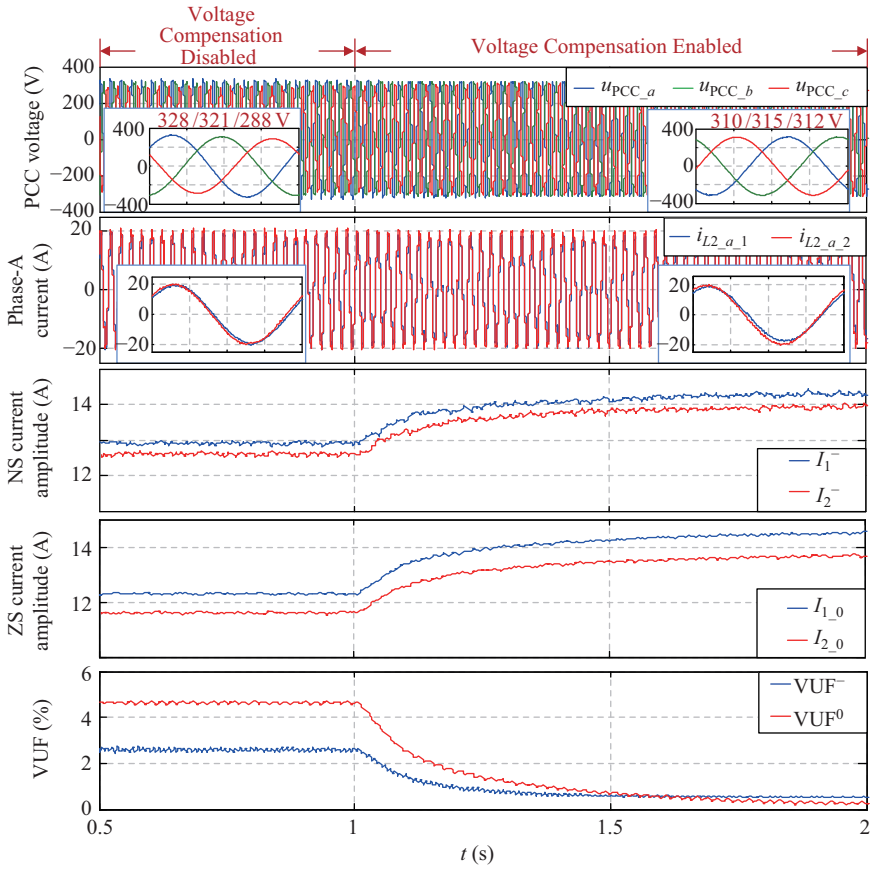


Fig. 15. Simulation results of case 2.

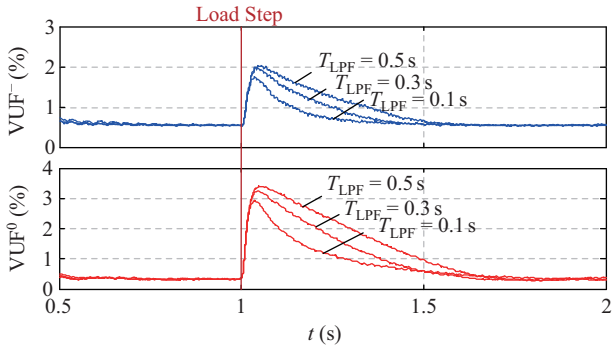


Fig. 16. Simulation results of case 3.

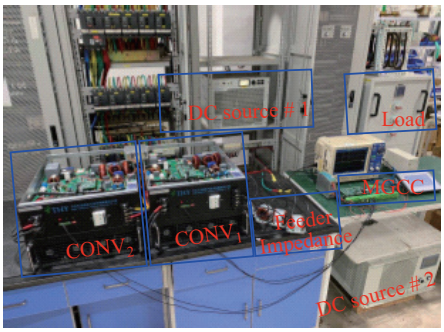


Fig. 17. Hardware setup.

the converters are shown in Fig. 18(a). It can be noted that the feeder impedance mismatch results in a current sharing error between the converters. Then, L_{v}^{+}, R_{v}^{-} and $R_{\mathrm{v\_0}}$ are set at 1 mH, 1 Ω and 2 Ω respectively. The amplitudes of PCC voltages (296/313/319 V) and three-phase output currents of the converters are shown in Fig. 18(b). It can be noted that sequence virtual impedance can improve the current sharing accuracy but causes amplitude deviation and imbalance in PCC voltage.

C. Experimental Case 2

The PCC voltage imbalance compensation method in Section IV is verified in case 2. L_{v}^{+}, R_{v}^{-} and $R_{\mathrm{v\_0}}$ are set at 1 mH, 1 Ω and 2 Ω respectively. Three-phase unbalanced loads, consisting of 8 kW in phase A, 3 kW in phase B and 3 kW in phase C, are supplied. The voltage imbalance compensation is enabled at t_1. As shown in Fig. 19, before the compensation is enabled, the amplitudes of PCC voltages are 296/320/319 V. After the compensation is enabled, the amplitudes of PCC voltages become 308/312/311 V. It can be concluded that the PCC voltage imbalance compensation method proposed in this paper rebalances the three-phase voltages toward their rated value. Meanwhile, the current sharing accuracy is guaranteed.

D. Experimental Case 3

The dynamics of the PCC voltage imbalance compensation method in Section IV are verified in case 3. First, L_{v}^{+}, R_{v}^{-} and $R_{\mathrm{v\_0}}$ are set at 1 mH, 1 Ω and 2 Ω respectively. PCC voltage compensation is enabled. Three-phase balanced loads, consisting of 3 kW per phase, are supplied before t_1 and then the phase-A load is increased by 5 kW at t_1. As shown in

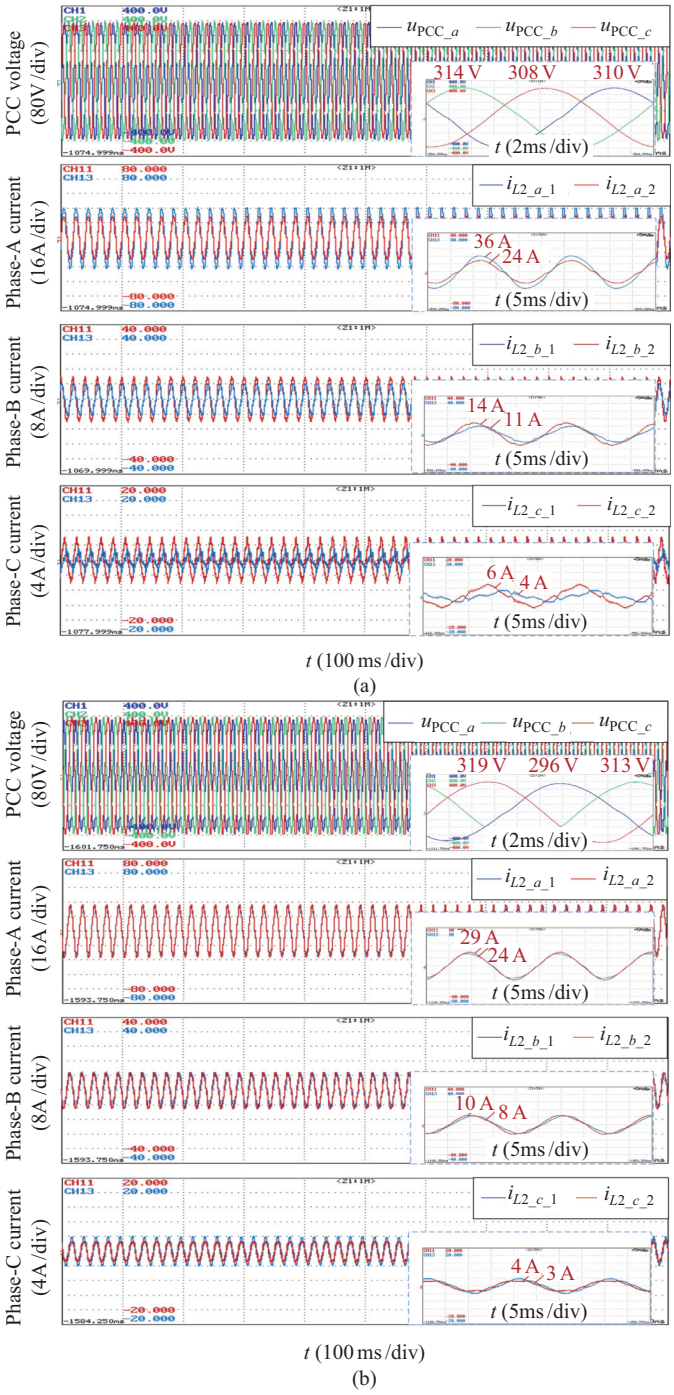


Fig. 18. Experimental results of case 1. (a) Without virtual sequence impedance. (b) With virtual sequence impedance inserted.

Fig. 20, after the load step, the amplitudes of PCC voltage recover from 295/319/314 V to 309/312/310 V within 0.5 s. Experimental results indicate that desired dynamics of the proposed PCC voltage compensation method can be achieved.

VII. Conclusion

This paper investigates the coordinated control of parallel 3P4W converters in AC MGs. The impact of virtual impedance on the accuracy of current sharing, PCC voltage quality and system stability are comprehensively and quantitatively

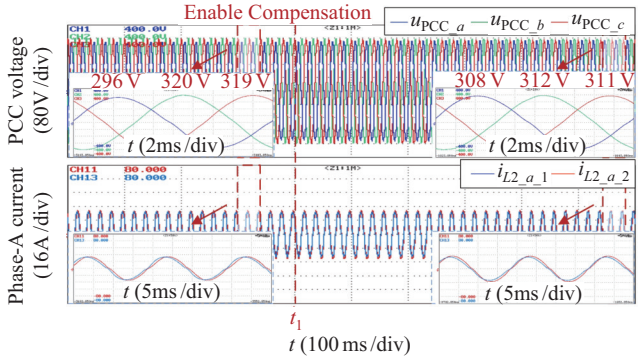


Fig. 19. Experimental results of case 2.

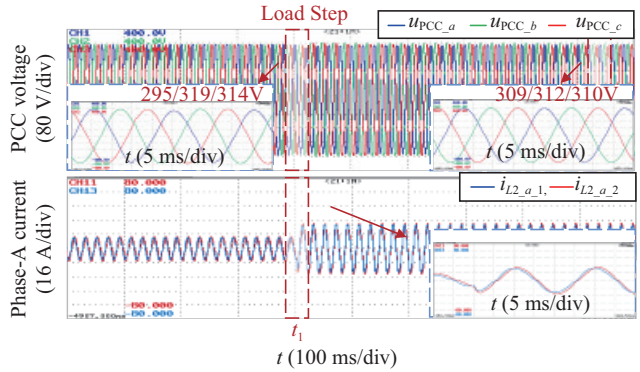


Fig. 20. Experimental results of case 3.

discussed. PS virtual inductance can enhance system stability and reduce the reactive power sharing error, but it increases the PCC voltage amplitude deviation. NS and ZS virtual inductances can reduce the NS and ZS current sharing error, but increase the NS and ZS components in PCC voltage. Constraints on the DC-link voltage should be satisfied to avoid over modulation when unbalanced loads are supplied.

To address the PCC voltage quality degradation caused by sequence virtual impedance, a PCC voltage imbalance compensation method based on LBC is proposed. The voltage compensation signals are transformed into DC quantities in the rotating reference frames for transmission. The tuning of related communication and control parameters are furnished. Simulation and experimental results show that the proposed method can compensate the PCC voltage while avoiding the impact on current sharing, with desirable dynamics.

However, the compensation of the three-sequence voltage components results in large amounts of variables to be transmitted in each communication cycle. How to optimize the transmission structure of the voltage compensation signals will be further studied.

APPENDIX

A. Derivation of Small Signal Model in (5).

In the PS circuit, the voltage, power and impedance of the system can be expressed by a complex number. For converter unit i, $U_{C\_i}e^{j\theta i}$ is the output voltage reference generated by droop control. S_i is the output complex power. $Y_{\text{load}}e^{j\varphi\text{load}}$ is the conductance of load. $Y_i e^{j\varphi i}$ is the conductance between filter capacitor C and PCC, which can be expressed as (A1).

$$Y_i e^{j\varphi_i} = 1/(R_{\text{v}}^{+} + j\omega L_{\text{v}}^{+} + j\omega L_2 + R_{\text{line\_}i} + j\omega L_{\text{line\_}i}) \tag{A1}$$

$U_{\text{PCC}}e^{j\theta\text{PCC}}$ is the PCC voltage, which can be expressed as:

$$U_{\text{PCC}}e^{j\theta\text{PCC}_{\text{PCC}}} = \frac{\sum_{i=1}^{n} Y_i e^{j\varphi i_i} U_{C\_i} e^{j\theta i_i}}{\sum_{i=1}^{n} Y_i e^{j\varphi i_i} + Y_{\text{load}} e^{j\varphi\text{load}_{\text{load}}}} \tag{A2}$$

S_i can be expressed as:

$$\begin{aligned}\overrightarrow{S}_i &= P_i + jQ_i \\ &= \left(\left(U_{C\_i}e^{j\theta_i} - U_{\text{PCC}}e^{j\theta_{\text{PCC}}}\right) Y_i e^{j\varphi_i}\right)^{*} U_{C\_i}e^{j\theta_i}\end{aligned} \tag{A3}$$

Using a system composed of two parallel converters for example, as shown in Fig. A1, by introducing a small disturbance $[\Delta\theta_1, \Delta\theta_2, \Delta U_{C\_1}, \Delta U_{C\_2}]^{\text{T}}$ to $U_{C\_i}e^{j\theta i}$ around the equilibrium point and combining (A1)-(A3) and (2), the characteristic equation of the PS circuit can be derived as (A4), where $\boldsymbol{E}$ is the identity matrix. Re and Im denote the real and imaginary parts of a complex number.

$$\begin{aligned}&\boldsymbol{G}^{+}\boldsymbol{X} = 0 \\ &\boldsymbol{X} = [\Delta\theta_1 \quad \Delta\theta_2 \quad \Delta U_{C\_1} \quad \Delta U_{C\_2}]^{\text{T}} \\ &\boldsymbol{G}^{+} = \boldsymbol{A}^{+} + \boldsymbol{B}^{+}\boldsymbol{C}^{+} \\ &\boldsymbol{A}^{+} = \begin{bmatrix} s(T_{PQ\_LPF}s+1)\boldsymbol{E}_{2\times2} & 0 \\ 0 & s(T_{PQ\_LPF}s+1)\boldsymbol{E}_{2\times2} \end{bmatrix} \\ &\boldsymbol{B}^{+} = \begin{bmatrix} k_{Pf}\boldsymbol{E}_{2\times2} & 0 \\ 0 & k_{QU}\boldsymbol{E}_{2\times2} \end{bmatrix} \\ &\boldsymbol{C}^{+} = \begin{bmatrix} \text{Re}\left(\frac{\partial\vec{S}_1}{\partial\theta_1}\right) & \text{Re}\left(\frac{\partial\vec{S}_1}{\partial\theta_2}\right) & \text{Re}\left(\frac{\partial\vec{S}_1}{\partial U_{C\_1}}\right) & \text{Re}\left(\frac{\partial\vec{S}_1}{\partial U_{C\_2}}\right) \\ \text{Re}\left(\frac{\partial\vec{S}_2}{\partial\theta_1}\right) & \text{Re}\left(\frac{\partial\vec{S}_2}{\partial\theta_2}\right) & \text{Re}\left(\frac{\partial\vec{S}_2}{\partial U_{C\_1}}\right) & \text{Re}\left(\frac{\partial\vec{S}_2}{\partial U_{C\_2}}\right) \\ \text{Im}\left(\frac{\partial\vec{S}_1}{\partial\theta_1}\right) & \text{Im}\left(\frac{\partial\vec{S}_1}{\partial\theta_2}\right) & \text{Im}\left(\frac{\partial\vec{S}_1}{\partial U_{C\_1}}\right) & \text{Im}\left(\frac{\partial\vec{S}_1}{\partial U_{C\_2}}\right) \\ \text{Im}\left(\frac{\partial\vec{S}_2}{\partial\theta_1}\right) & \text{Im}\left(\frac{\partial\vec{S}_2}{\partial\theta_2}\right) & \text{Im}\left(\frac{\partial\vec{S}_2}{\partial U_{C\_1}}\right) & \text{Im}\left(\frac{\partial\vec{S}_2}{\partial U_{C\_2}}\right) \end{bmatrix}\end{aligned} \tag{A4}$$

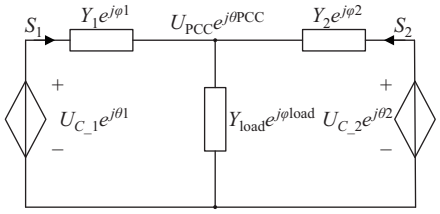


Fig. A1. PS equivalent circuit.

B. Expression of (8).

In (8), $\boldsymbol{G}_1^{-}$, $\boldsymbol{G}_2^{-}$ and $\boldsymbol{Z}^{-}$ can be expressed as

$$\begin{aligned}\boldsymbol{G}_1^{-} &= (\boldsymbol{Z}_{\text{line\_1}} + \boldsymbol{Z}_{\text{inv1}}^{-})(\boldsymbol{Z}_{\text{line\_1}} + \boldsymbol{Z}_{\text{inv1}}^{-} + \boldsymbol{Z}_{\text{line\_2}} + \boldsymbol{Z}_{\text{inv2}}^{-})^{-1} \\ &\quad \times (\boldsymbol{Z}_{\text{line\_2}} + \boldsymbol{Z}_{\text{inv2}}^{-})(\boldsymbol{Z}_{\text{line\_1}} + \boldsymbol{Z}_{\text{inv1}}^{-})^{-1}\boldsymbol{G}_{\text{inv1}}^{-} \\ \boldsymbol{G}_2^{-} &= (\boldsymbol{Z}_{\text{line\_1}} + \boldsymbol{Z}_{\text{inv1}}^{-}) \\ &\quad \times (\boldsymbol{Z}_{\text{line\_1}} + \boldsymbol{Z}_{\text{inv1}}^{-} + \boldsymbol{Z}_{\text{line\_2}} + \boldsymbol{Z}_{\text{inv2}}^{-})^{-1}\boldsymbol{G}_{\text{inv2}}^{-} \\ \boldsymbol{Z}^{-} &= -(\boldsymbol{Z}_{\text{line\_1}} + \boldsymbol{Z}_{\text{inv1}}^{-})(\boldsymbol{Z}_{\text{line\_1}} + \boldsymbol{Z}_{\text{inv1}}^{-} + \boldsymbol{Z}_{\text{line\_2}} + \boldsymbol{Z}_{\text{inv2}}^{-})^{-1} \\ &\quad \times (\boldsymbol{Z}_{\text{line\_2}} + \boldsymbol{Z}_{\text{inv2}}^{-})\end{aligned} \tag{A5}$$

where

$$\boldsymbol{Z}_{\text{line\_1}}=\begin{bmatrix} Z_{\text{line\_1}} & 0 \\ 0 & Z_{\text{line\_1}} \end{bmatrix}, \boldsymbol{Z}_{\text{line\_2}}=\begin{bmatrix} Z_{\text{line\_2}} & 0 \\ 0 & Z_{\text{line\_2}} \end{bmatrix} \tag{A6}$$

$$\boldsymbol{Z}^{-}_{\text{inv1/inv2}}=\begin{bmatrix} Z^{-}_{\alpha\alpha} & Z^{-}_{\alpha\beta} \\ Z^{-}_{\beta\alpha} & Z^{-}_{\beta\beta} \end{bmatrix}, \boldsymbol{G}^{-}_{\text{inv1/inv2}}=\begin{bmatrix} G^{-}_{\alpha\alpha} & 0 \\ 0 & G^{-}_{\beta\beta} \end{bmatrix} \tag{A7}$$

$$\begin{aligned}
Z^{-}_{\alpha\alpha} &= \frac{L_1 s+\frac{1}{2}(R^{-}_{\text{v}}D-\omega L^{-}_{\text{v}}Q)}{\begin{array}{c}L_1Cs^2+(CG_iG_{\text{PWM}}+CR_{\text{d}})s \\ +G_{v_\text{PR}}G_iG_{\text{PWM}}-G_{\text{PWM}}+1\end{array}}+L_2 s \\
Z^{-}_{\beta\beta} &= \frac{L_1 s+\frac{1}{2}(R^{-}_{\text{v}}D-\omega L^{-}_{\text{v}}Q)}{\begin{array}{c}L_1Cs^2+(CG_iG_{\text{PWM}}+CR_{\text{d}})s \\ +G_{v_\text{PR}}G_iG_{\text{PWM}}-G_{\text{PWM}}+1\end{array}}+L_2 s \\
Z^{-}_{\alpha\beta} &= \frac{\frac{1}{2}(R^{-}_{\text{v}}Q+\omega L^{-}_{\text{v}}D)G_{v_\text{PR}}G_iG_{\text{PWM}}}{\begin{array}{c}L_1Cs^2+(CG_iG_{\text{PWM}}+CR_{\text{d}})s \\ +G_{v_\text{PR}}G_iG_{\text{PWM}}-G_{\text{PWM}}+1\end{array}} \\
Z^{-}_{\beta\alpha} &= \frac{\frac{1}{2}(-R^{-}_{\text{v}}Q-\omega L^{-}_{\text{v}}D)G_{v_\text{PR}}G_iG_{\text{PWM}}}{\begin{array}{c}L_1Cs^2+(CG_iG_{\text{PWM}}+CR_{\text{d}})s \\ +G_{v_\text{PR}}G_iG_{\text{PWM}}-G_{\text{PWM}}+1\end{array}} \\
G^{-}_{\alpha\alpha} &= G^{-}_{\beta\beta}=\frac{G_{v_\text{PR}}G_iG_{\text{PWM}}}{\begin{array}{c}L_1Cs^2+(CR_{\text{d}}+CG_iG_{\text{PWM}})s \\ +G_{v_\text{PR}}G_iG_{\text{PWM}}-G_{\text{PWM}}+1\end{array}}
\end{aligned} \tag{A8}$$

The expression of D and Q in (A7) can be found in [28].

C. Expression of (12)

In (12), G_{0_1}, G_{0_2} and Z_0 can be expressed as:

$$\begin{aligned}
G_{0_1} &= \frac{(Z_{\text{line_2}}+Z_{\text{inv2_0}})G_{\text{inv1_0}}}{Z_{\text{line_1}}+Z_{\text{inv1_0}}+Z_{\text{line_2}}+Z_{\text{inv2_0}}} \\
G_{0_2} &= \frac{(Z_{\text{line_1}}+Z_{\text{inv1_0}})G_{\text{inv2_0}}}{Z_{\text{line_1}}+Z_{\text{inv1_0}}+Z_{\text{line_2}}+Z_{\text{inv2_0}}} \\
Z_0 &= -\frac{(Z_{\text{line_1}}+Z_{\text{inv1_0}})(Z_{\text{line_2}}+Z_{\text{inv2_0}})}{Z_{\text{line_1}}+Z_{\text{inv1_0}}+Z_{\text{line_2}}+Z_{\text{inv2_0}}}
\end{aligned} \tag{A9}$$

where

$$\begin{aligned}
Z_{\text{inv1/inv2_0}} &= \frac{(L_1+3L_n)s+R_{\text{v0}}G_{v_\text{PR}}G_iG_{\text{PWM}}+G_iG_{\text{PWM}}}{\begin{array}{c}(L_1+3L_n)Cs^2+(CG_iG_{\text{PWM}}+CR_{\text{d}})s \\ +G_{v_\text{PR}}G_iG_{\text{PWM}}-G_{\text{PWM}}+1\end{array}} \\
&\quad + L_2 s \\
G_{\text{inv1/inv2_0}} &= \frac{G_{v_\text{PR}}G_iG_{\text{PWM}}}{\begin{array}{c}(L_1+3L_n)Cs^2+(CR_{\text{d}}+CG_iG_{\text{PWM}})s \\ +G_{v_\text{PR}}G_iG_{\text{PWM}}-G_{\text{PWM}}+1\end{array}}
\end{aligned} \tag{A10}$$

D. Derivation of (19).

According to Fig. 11, the closed-loop transfer function diagram of PS voltage compensation in AC MG composed of two parallel converters can be illustrated as Fig. A2, where $\partial U_{\text{PCC}}/\partial U_{C\_1}$, $\partial U_{\text{PCC}}/\partial U_{C\_2}$ and $\partial U_{\text{PCC}}/\partial Y_{\text{load}}$ can be obtained from (A2). Given $Y_1 e^{j\varphi 1}=Y_2 e^{j\varphi 2}$, the transfer function from ΔY_{load} to ΔU_{PCC} can be expressed as:

$$\Delta U_{\text{PCC}}=\frac{\partial U_{\text{PCC}}/\partial Y_{\text{load}}}{\left(2\frac{\partial U_{\text{PCC}}}{\partial U_{C\_1}}G_{\text{com}}G_{\text{LPF}}G_{\text{CAN}}+1\right)}\Delta Y_{\text{load}} \tag{A11}$$

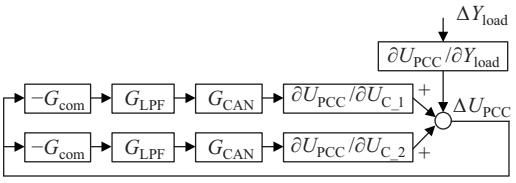


Fig. A2. Transfer function diagram of PS voltage compensation.

Transforming (9) into rotating reference frame with angular frequency $-\omega$, (A11) can be obtained. According to Fig. 11, the closed-loop transfer function diagram of NS voltage compensation in AC MG composed of two parallel converters can be illustrated as Fig. A3.

$$u^{-}_{\text{PCC\_}dq}=\frac{1}{2}u^{-}_{\text{1\_com\_}dq}+\frac{1}{2}u^{-}_{\text{2\_com\_}dq}-\frac{R^{-}_{\text{v}}}{2}i^{-}_{L2\_dq} \tag{A12}$$

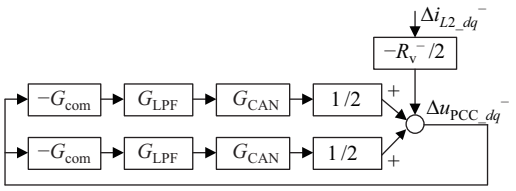


Fig. A3. Transfer function diagram of NS voltage compensation.

The transfer function from $\Delta i^{-}_{L2\_dq}$ to $\Delta u^{-}_{\text{PCC\_}dq}$ can be expressed as:

$$\Delta u^{-}_{\text{PCC\_}dq}=\frac{-R^{-}_{\text{v}}}{2(G_{\text{com}}G_{\text{LPF}}G_{\text{CAN}}+1)}\Delta i^{-}_{L2\_dq} \tag{A13}$$

Transforming (13) into a rotating reference frame with angular frequency ω, (A13) can be obtained. According to Fig. 11, the closed-loop transfer function diagram of NS voltage compensation in AC MG composed of two parallel converters can be illustrated as Fig. A4.

$$u_{\text{PCC\_}dq\_0}=\frac{1}{2}u_{\text{1\_com\_}dq\_0}+\frac{1}{2}u_{\text{1\_com\_}dq\_0}-\frac{R_{\text{v\_0}}}{2}i_{L2\_dq\_0} \tag{A14}$$

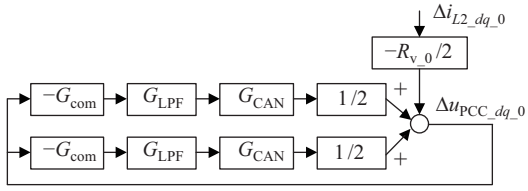


Fig. A4. Transfer function diagram of ZS voltage compensation.

The transfer function from $\Delta i_{L2\_dq\_0}$ to $\Delta u_{\text{PCC\_}dq\_0}$ can be expressed as:

$$\Delta u_{\text{PCC\_}dq\_0}=\frac{-R_{\text{v\_0}}}{2(G_{\text{com}}G_{\text{LPF}}G_{\text{CAN}}+1)}\Delta i_{L2\_dq\_0} \tag{A15}$$

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Rui Liu received the B.S. degree from China Agricultural University, Beijing, China, in 2018, and the M.S. degree from Tianjin University, Tianjin, China, in 2021, both in Electrical Engineering. His research interest includes modeling and control of AC microgrids.

Li Guo received B.Sc. and Ph.D. degrees in Electrical Engineering from South China University of Technology, Guangzhou, China, in 2002 and 2007, respectively. He is currently a Full Professor with Tianjin University, Tianjin, China. His research interests include the optimal planning and design of microgrids, the coordinated operating strategy of microgrids, and advanced energy management systems.

Xialin Li received B.Sc. and Ph.D. degrees in Electrical Engineering from Tianjin University, Tianjin, China, in 2009 and 2014, respectively. In 2016, under the State Scholarship Fund, he was invited as a Visiting Professor to the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. Since 2018, he has been an Associate Professor with the School of Electrical Engineering and Automation, Tianjin University. His research interests include the modeling and control of power converters, distributed generation, hybrid AC-DC microgrids, and multiterminal DC grids.