Time-delay Correction Control Strategy for HVDC Frequency Regulation Services

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***Abstract*—With the advancements in voltage source converter (VSC) technology, VSC based high voltage direct current (VSC-HVDC) systems provide system operators with a prospective approach to enhance system operating stability and resilience. In addition to long-distance transmission, the VSC-HVDC system can also provide multiple ancillary services, such as frequency regulation, due to its power controllability. However, if a time delay exists in the control signal, the VSC-HVDC system may bring destabilizing influences to the system, which will decrease the system resilience under the disturbance. In order to reduce control deviation caused by time delay, in this paper, a small signal model is first conducted to analyze the impact of time delay on system stability. Then a time-delay correction control strategy for HVDC frequency regulation control is developed to reduce the influence of the time delay. The control performance of the proposed time-delay correction control is verified both in the established small signal model and the runtime simulation in a modified IEEE 39 bus system. The results indicate that the proposed time-delay correction control strategy shows significant improvement in system stability.**

***Index Terms*—Frequency regulation control, HVDC, small signal analysis, time delay, time-delay correction control strategy.**

NOMENCLATURE

A. Parameters

T_d, T_s	Delay time and sampling time for PMU.
$f_{\rm ref}$, ω_0	Nominal frequency and rotor speed.
$k_{\rm pf}$, $k_{\rm if}$	Proportional and integral constant for HVDC frequency regulation control.
$P_{\rm ref}$, $Q_{\rm ref}$	Reference value for real and reactive power.
$k_{\rm pp}$, $k_{\rm ip}$	Proportional and integral constant for outer loop real power control.
$k_{\rm pq}$, $k_{\rm iq}$	Proportional and integral constant for outer loop reactive power control.
$k_{\rm pid}$, $k_{\rm iid}$	Proportional and integral constant for inner loop d-axis current control.
$k_{\rm piq}$, $k_{\rm iiq}$	Proportional and integral constant for inner loop q-axis current control.
$k_{\rm pPLL}$, $k_{\rm iPLL}$	Proportional and integral constant for PLL.
L_f	Transformer inductance.
T_J	Inertia time constant.
D	Damping coefficient.

B. Variables

$f_{\rm PMU}$	Measured frequency from PMU.
$f_{\rm PMU}^{\rm td}$	Measured frequency received at controller after time delay.
P_s, Q_s	Measured HVDC real and reactive power.
P_m	Total active power input of outer loop active power control.
$i_{\rm sdref}$, $i_{\rm sqref}$	Reference value for d/q-axis AC current.
$u_{\rm cd}$, $u_{\rm cq}$	d/q-axis AC voltage at converter.
$u_{\rm sd}$, $u_{\rm sq}$	d/q-axis voltage at PCC point.
$i_{\rm sd}$, $i_{\rm sq}$	d/q-axis current.
ω, θ_p	Rotor angular speed and phase angle at PCC point.
δ, ω_g	Rotor position angle and rotor speed of the generator.
E'_d, E'_q	d/q-axis electromotive force in the equivalent generator function.
$P_{\rm mc}$, $P_{\rm e}$	Mechanical/electrical power of generator.

I. INTRODUCTION

WITH the increasing penetration of renewable energies into power systems, such as wind, hydro and solar power, the generation mix allows for rapid change in recent years [1], [2]. Conventional fossil fuel generation plants are being pushed off the power grid due to their emission reduction requirements [3]. On the contrary, renewable energy generation witnesses continuous growth during the decade due to the increasing maturity of the technology and decreasing investment expenses [4]. According to a recent IEA report, although the supply chain and construction planning are influenced by the coronavirus, the total global use of renewable energies may still increase by about 1% and reach a new record in 2020 [5].

However, there are two differences between the traditional generation and renewable energies that may bring significant effects to the power system operations. First, the planning of the renewable energy plants must depend on the geographical distribution of renewable energies [4]. Thus, most renewable energy plants are constructed in sparsely populated regions.

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The electrical network structures in these regions are not strong enough so that the delivery and management of the renewable energy generation becomes an issue to the system operators. Secondly, some types of renewable energies, represented by wind and solar energy, are usually connected to the power system via grid-connected converters (GCCs). Different from the traditional generators and motors, renewable energies integrating into power systems with GCCs do not provide inertia [6]. Therefore, the system inertia is unavoidably decreased with the accelerated penetration of renewable energies. The power system with high proportional renewable generation will be more vulnerable under disturbances, which brings more challenges to system operation reliability.

The advancement of the voltage source converter based high voltage direct current (VSC-HVDC) system provides the system operators with a prospective way to enhance system operating stability and resilience [7]–[12]. The HVDC transmission system has been widely used in bulk power transporting over long distances [13]. With the increasing number of offshore windfarms and the promotion of super grid plans in Europe and China, the HVDC system addresses an unprecedented developing period [14]–[16]. According to [17], the global HVDC system may achieve a compound annual growth rate (CAGR) of 11.18% from 2020 to 2025. In addition to long-distance transmission, the HVDC system could also provide multiple ancillary services, such as inertia emulation, frequency regulation, and oscillation suppression [18]. Compared to other services, frequency regulation is regarded as one of the most valuable additional products of the HVDC system [19], which has been investigated by some academics and industries. Some frequency regulation control strategies based on the HVDC system were also developed [20]–[24].

However, most of the control strategies do not consider the time-delay influence of the signal transmission loop. The time-delay will occur in the measurement process [25], the communication process between PMU and control center [26], etc. In analysis, the delay in multiple parts can be represented by a single time delay in the control loop [27]. With the increase of the scale and complexity of the electric power network, the local information based HVDC controller is not appropriate for HVDC transmission systems with new control requirements. The wide-area monitoring system (WAMS) based HVDC control becomes mainstream. The time delay is inevitable due to the time consumption of the measurement, calculation, and communications. Depending on the different communication distances, and protocol and performance of measuring devices, the time delay may vary from tens to hundreds of milliseconds (ms) [28]. Due to the fast power controllability, the time delay of the control signal in the HVDC frequency control may bring more destabilizing influences to the system than other devices, which will decrease the resilience under the disturbance. There are some researchers who have studied the time-delay effect on the HVDC system, and some control strategies have been proposed to deal with this issue [28]–[32]. In [29], the impact of time delay on wide-area controller design in power systems is analyzed, and a centralized wide-area controller design is proposed to enhance the stability of the system under time-delay conditions. In [30], a damping control design is proposed that uses the improved Smith Predictor Control to consider the time-delay effect of the feedback signals. In [28], [31] and [32], some damping controllers with different principles are proposed for the WAMS based HVDC systems to suppress the oscillation caused by time delays. However, the time-delay correction method commonly employed in power systems is the lead-lag structure, which is only suitable for oscillation-related issues and not applicable for frequency drops. Moreover, most of the developed correction methods are based on known system models. The actual system is under continuous adjustments, with different types of generators and load puts, impacting the operation or retirement. The model-based methods may have some limitations and are not appropriate for the current developing power systems.

The main objective of this paper is to develop a correction control strategy HVDC frequency regulation service, so as to reduce the control deviation caused by time delay. The development of this method includes the following procedures:

1) Establish a small signal model. The small signal model is utilized to analyze the impact of the time delay on system stability.

2) Raise the correction control strategy. To reduce the risk of system instability caused by the time delay, a model-free correction control is proposed which only needs the measured frequency data.

3) Verify the control performance. For comprehensive verification, the control effect will be tested by both small signal analysis and runtime simulations.

The remainder of this paper is organized as follows. Section II introduces the time-delay influences on the HVDC frequency regulation control and establishes a small signal model to quantitatively analyze the time-delay impact on HVDC control. Section III describes the principle of the proposed time-delay correction control strategy for the HVDC frequency regulation service. Section IV verifies the control performance of the proposed time-delay correction control with an established small signal model and a modified IEEE 39 bus system. The paper is concluded in Section V.

II. Communication Delay Analysis based Small Signal Model

A. Communication Delay During the HVDC Control Process

The conventional frequency regulation service of the HVDC system is performed based on the control framework, as shown in Fig. 1. The corresponding control process can be described.

The frequency regulation service of the HVDC system is based on the measured frequency and phase angles via phase measured units (PMUs). When the data is obtained, the PMUs will send the measured data to the Phase Data Concentrators (PDC) server, generally via communication protocol IEEE C37.118 [33]. After receiving the data, the PDC will send the data to the HVDC frequency regulation control. The HVDC frequency regulation control will calculate the control order by measured frequency, and then send it to the basic HVDC control to regulate the power flow so as to realize the frequency regulation of the AC system.

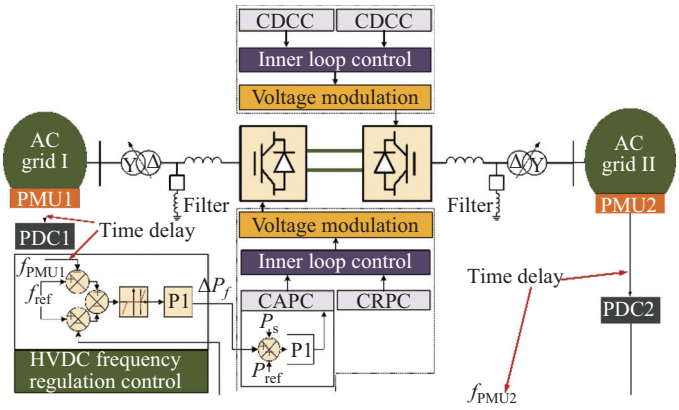

Fig. 1. The control framework of the HVDC system, where f_{ref} is the nominal frequency, the $f_{\mathrm{PMU1}}/f_{\mathrm{PMU2}}$ are the frequencies measured from AC grid I and AC grid II, the P_s is the real-time power flow on the HVDC system and the P_{ref} is the active power reference of the HVDC system. CDCC refers to constant DC voltage control, CAPC is the constant active power control and CRPC is constant reactive power control.

In the practical system operations, as shown in Fig. 1, due to the communication time delay from the PMU to PDC, or from PDC to the controller, and the operational time delay, the signal time delay in the HVDC control system is inevitable. In [34], the Ontario system operator reports that a one-way delay may be up to 4 seconds. If this long-term time delay occurs in the HVDC control process, the control performance of the HVDC system could be significantly impacted. Moreover, the delayed response of the HVDC system may bring serious disturbances so as to reduce the system stability and introduce oscillation, which will have negative influence on the system's resilience.

B. Small Signal Modeling for HVDC Considering Time Delay

In this section, for quantitatively analyzing the control signal time-delay influence on the HVDC system control, a small signal model is established. In order to focus on the impact of time delay on system stability while simplifying the model, a one-terminal VSC system connected with a generator is adopted as the small signal test system. In the VSC small signal model, the control diagram is shown in Fig. 2, including frequency regulation control with time delay, outer loop control, inner loop control, and the phase-locked loop (PLL). The stability analysis is performed using MATLAB R2019b. Each component of the VSC small signal model is described as follows.

1) Frequency Regulation Control with Time Delay

The time delay generated from PMU or PDC will impact the measured frequency. According to [35], the fourth-order Pade approximation model can accurately describe the time delay characteristics, which can be expressed as:

$$\begin{aligned}\frac{f_{\mathrm{PMU}}^{\mathrm{td}}}{f_{\mathrm{PMU}}} &= e^{-sT_d} \\ &\approx \frac{(T_d s)^4 - 20(T_d s)^3 + 180(T_d s)^2 - 840(T_d s) + 1680}{(T_d s)^4 + 20(T_d s)^3 + 180(T_d s)^2 + 840(T_d s) + 1680}\end{aligned} \tag{1}$$

Based on modern control theory, the Pade approximation transfer function can be converted into state space expressions as:

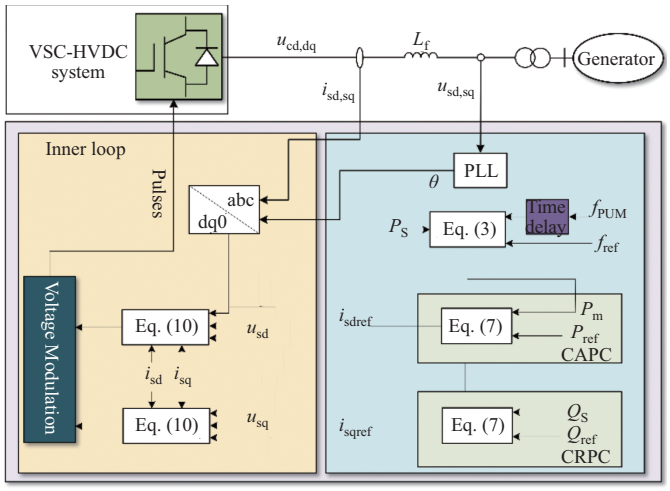

Fig. 2. The control diagram of the test system.

$$\begin{cases}\dfrac{\mathrm{d}}{\mathrm{d}t} z_p = A_p z_p + B_p u_p \\ y_p = C_p z_p + D_p u_p\end{cases} \tag{2}$$

where the state variable matrix $z_p = [z_1 z_2 z_3 z_4]^{\mathrm{T}}$; the input variable $u_p = f_{\mathrm{PMU}}$; the output variable $y_p = f_{\mathrm{PMU}}^{\mathrm{td}}$. z_1, z_2, z_3 and z_4 are four state variables introduced by the Pade approximation link.

After linearization, the small signal of the delayed frequency $f_{\mathrm{PMU}}^{\mathrm{td}}$ can be written as:

$$\begin{aligned}\Delta f_{\mathrm{PMU}}^{\mathrm{td}} &= -\frac{40}{T_d}\Delta z_1 - \frac{1680}{T_d^3}\Delta z_3 + \Delta f_{\mathrm{PMU}} \\ &= -\frac{40}{T_d}\Delta z_1 - \frac{1680}{T_d^3}\Delta z_3 + \frac{1}{2\pi}\Delta\omega_g\end{aligned} \tag{3}$$

The difference between the measured frequency after time delay and the nominal frequency will go through the frequency regulation control, which can be considered as a proportional and integral (PI) controller. The output of the frequency regulation control is then added to the active power as the input of the outer loop control. The linearized function is described as:

$$\Delta P_m = \left(k_{\mathrm{pf}} + \frac{k_{\mathrm{if}}}{s}\right)(\Delta f_{\mathrm{ref}} - \Delta f_{\mathrm{PMU}}^{\mathrm{td}}) + \Delta P_s \tag{4}$$

In order to eliminate the influence of the integral part in (4), an intermediate state variable x_f is introduced, as:

$$\frac{\mathrm{d}}{\mathrm{d}t}\Delta x_f = \frac{40}{T_d}\Delta z_1 + \frac{1680}{T_d^3}\Delta z_3 - \frac{1}{2\pi}\Delta\omega_g \tag{5}$$

Substituting (5) into (4), then ΔP_m can be expressed as:

$$\begin{aligned}\Delta P_m = &\frac{40}{T_d}k_{\mathrm{pf}}\Delta z_1 + \frac{1680}{T_d^3}k_{\mathrm{pf}}\Delta z_3 - \frac{1}{2\pi}k_{\mathrm{pf}}\Delta\omega_g \\ &+ k_{\mathrm{if}}\Delta x_f + \Delta P_s\end{aligned} \tag{6}$$

2) Outer Loop Control

The objective of the outer loop control is to control the active power and reactive power. The main structure of the outer loop control comprises two independent PI controllers, with P_m and Q_s in the track of their respective reference values. The outputs of the outer loop control are the current reference value in the dq frame, which will be fed into the inner loop current control. The dynamic functions for the outer loop control can be expressed as:

$$\begin{cases} i_{\mathrm{sdref}} = (P_{\mathrm{ref}} - P_m)\left(k_{\mathrm{pp}} + \dfrac{k_{\mathrm{ip}}}{s}\right) \\ i_{\mathrm{sqref}} = (Q_{\mathrm{ref}} - Q_s)\left(k_{\mathrm{pq}} + \dfrac{k_{\mathrm{iq}}}{s}\right) \end{cases} \tag{7}$$

The intermediate state variables ϕ_p, ϕ_q are introduced to represent the integral part of the input difference of the outer loop control, as:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\phi_p \\ \phi_q\end{bmatrix} = \begin{bmatrix}k_{\mathrm{ip}} & 0 \\ 0 & k_{\mathrm{iq}}\end{bmatrix}\begin{bmatrix}P_{\mathrm{ref}} \\ Q_{\mathrm{ref}}\end{bmatrix} + \begin{bmatrix}-k_{\mathrm{ip}} & 0 \\ 0 & -k_{\mathrm{iq}}\end{bmatrix}\begin{bmatrix}P_m \\ Q_s\end{bmatrix} \tag{8}$$

Then (7) can be represented by the intermediate state variables ϕ_p and ϕ_q:

$$\begin{bmatrix}i_{\mathrm{sdref}} \\ i_{\mathrm{sqref}}\end{bmatrix} = \begin{bmatrix}\phi_p \\ \phi_q\end{bmatrix} + \begin{bmatrix}k_{\mathrm{pp}} & 0 \\ 0 & k_{\mathrm{pq}}\end{bmatrix}\begin{bmatrix}P_{\mathrm{ref}} \\ Q_{\mathrm{ref}}\end{bmatrix} + \begin{bmatrix}-k_{\mathrm{pp}} & 0 \\ 0 & -k_{\mathrm{pq}}\end{bmatrix}\begin{bmatrix}P_m \\ Q_s\end{bmatrix} \tag{9}$$

3) Inner Loop Control

The output of the inner loop control is the VSC reference voltage value in the dq frame, which is finally fed into the PWM module to generate gate pulses for VSC power electronic switches. The dynamic functions for inner loop control can be expressed as:

$$\begin{cases} u_{\mathrm{cd}} = u_{\mathrm{sd}} - (i_{\mathrm{sdref}} - i_{\mathrm{sd}})\left(k_{\mathrm{pid}} + \dfrac{k_{\mathrm{iid}}}{s}\right) - \omega L_f i_{\mathrm{sq}} \\ u_{\mathrm{cq}} = u_{\mathrm{sq}} - (i_{\mathrm{sqref}} - i_{\mathrm{sq}})\left(k_{\mathrm{piq}} + \dfrac{k_{\mathrm{iiq}}}{s}\right) + \omega L_f i_{\mathrm{sd}} \end{cases} \tag{10}$$

Similarly, intermediate state variables ϕ_{id} and ϕ_{iq} can be introduced to represent the integral part of the input difference of the inner loop control, as in (11):

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\phi_{\mathrm{id}} \\ \phi_{\mathrm{iq}}\end{bmatrix} = \begin{bmatrix}k_{\mathrm{iid}} & 0 \\ 0 & k_{\mathrm{iiq}}\end{bmatrix}\begin{bmatrix}i_{\mathrm{sdref}} \\ i_{\mathrm{sqref}}\end{bmatrix} + \begin{bmatrix}-k_{\mathrm{iid}} & 0 \\ 0 & -k_{\mathrm{iiq}}\end{bmatrix}\begin{bmatrix}i_{\mathrm{sd}} \\ i_{\mathrm{sq}}\end{bmatrix} \tag{11}$$

Then (10) can be represented by the intermediate state variables ϕ_{id} and ϕ_{iq}:

$$\begin{bmatrix}u_{\mathrm{cd}} \\ u_{\mathrm{cq}}\end{bmatrix} = \begin{bmatrix}u_{\mathrm{sd}} \\ u_{\mathrm{sq}}\end{bmatrix} - \begin{bmatrix}\phi_{\mathrm{id}} \\ \phi_{\mathrm{iq}}\end{bmatrix} - \begin{bmatrix}k_{\mathrm{pid}} & 0 \\ 0 & k_{\mathrm{piq}}\end{bmatrix}\begin{bmatrix}i_{\mathrm{sdref}} \\ i_{\mathrm{sqref}}\end{bmatrix} + \begin{bmatrix}k_{\mathrm{pid}} & -\omega L_f \\ \omega L_f & k_{\mathrm{piq}}\end{bmatrix}\begin{bmatrix}i_{\mathrm{sd}} \\ i_{\mathrm{sq}}\end{bmatrix} \tag{12}$$

4) Phase-Locked Loop (PLL)

The real-time frequency at PCC is measured by the PLL block, which consists of a PI controller to track u_{sq} to zero. The dynamic function of PLL is represented as:

$$\theta_p = \frac{1}{s}[(k_{\mathrm{pPLL}} + k_{\mathrm{iPLL}})u_{\mathrm{sq}} + \omega_0] \tag{13}$$

The intermediate state variable ϕ_p is introduced to eliminate integral operator s, so the equation (13) can be rewritten as:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\phi_p \\ \theta_p\end{bmatrix} = \begin{bmatrix}0 & 0 \\ 1 & 0\end{bmatrix}\begin{bmatrix}\phi_p \\ \theta_p\end{bmatrix} + \begin{bmatrix}0 & k_{\mathrm{iPLL}} \\ 0 & k_{\mathrm{pPLL}}\end{bmatrix}\begin{bmatrix}u_{\mathrm{sd}} \\ u_{\mathrm{sq}}\end{bmatrix} + \begin{bmatrix}0 \\ \omega_0 t\end{bmatrix} \tag{14}$$

5) Generator

Since only focusing on the frequency characteristics in the power system, the electromagnetic transient characteristics can be ignored when modeling. The classical second-order model is applied to represent the generator, which only considers the rotor motion of the generator. The dynamic functions for the generator are expressed as:

$$\begin{cases} \dfrac{\mathrm{d}\delta}{\mathrm{d}t} = \omega_g - \omega_0 \\ T_J \dfrac{\mathrm{d}\omega_g}{\mathrm{d}t} = P_{\mathrm{mc}} - P_{\mathrm{e}} - D\omega_g \end{cases} \tag{15}$$

In the small signal test system with one generator, the measured frequency from PMU in (1) can be considered the same as the generator frequency, which indicates that:

$$\omega_g = 2\pi f_{\mathrm{PMU}} \tag{16}$$

6) Small Signal Modeling

Since eigenvalue analysis, by using state space modeling, is one of the best methods to analyze the system stability, all the state space functions should be represented in first-order differential equations, as shown in (2), (5), (8), (11), (14) and (15).

Based on the state space functions, the small signal state space model can be obtained by linearizing (2), (8), (9), (11), (12), and (14)–(16), together with (5)–(6), expressed as:

$$\frac{\mathrm{d}\Delta \boldsymbol{x}}{\mathrm{d}t} = \boldsymbol{A}\Delta \boldsymbol{x} + \boldsymbol{B}\Delta \boldsymbol{u} \tag{17}$$

where the small signal of state variables of the system is represented by vector $\boldsymbol{x}$, while the small signal of input variables is represented by vector $\boldsymbol{u}$. $\boldsymbol{A}$ is the state matrix containing system stability information, which can be used to calculate the system eigenvalue. $\boldsymbol{B}$ is the input matrix.

In this test system, $\boldsymbol{x} = [\delta,\ \phi_p,\ \phi_q,\ \phi_{\mathrm{id}},\ \phi_{\mathrm{iq}},\ \omega_g,\ z_1,\ z_3,\ x_f,\ z_2,\ z_4,\ \phi_p,\ \theta_p]^{\mathrm{T}}$, $\boldsymbol{u} = [P_{\mathrm{ref}}, Q_{\mathrm{ref}}]$, $\boldsymbol{A}$ is a 13 × 13 matrix while $\boldsymbol{B}$ is a 13 × 2 matrix.

Figure 3 shows the eigenvalue locus of $\boldsymbol{A}$ with time delay T_d varying from 20 ms to 300 ms. In this simulation, the system operates at a rated state and all the other system parameters remain unchanged.

As shown in Fig. 3, the eigenvalue of the dominant mode moves to the positive direction of the real axis with T_d increasing. The dominant mode refers to the set of conjugate eigenvalues whose real part first changes from negative to positive among all sets of eigenvalues when system parameters vary. It is also the key mode to cause system instability. When the time delay is larger than 142 ms, the eigenvalue will reach the right half plane of the coordinate axis, which

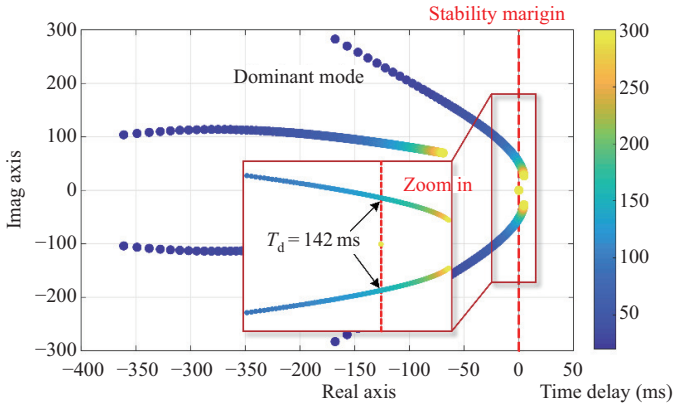

Fig. 3. The eigenvalue locus with time delay varying from 20 ms to 300 ms.

indicates that the system becomes unstable. It can be seen from the results that, with the increase of control time delay in the HVDC system, the small signal stability margin is reduced, and system instability even occurs. Therefore, how to mitigate the influence of time delay on system stability is an intractability problem that needs to be well studied and addressed.

III. Time-delay Correction Control Strategy

The principle of time delay in frequency measurement is shown in Fig. 4, where the frequency deviation of the actual signal, which is also considered as the "sending signal", is represented by the dark blue curve, while the light blue line is the frequency deviation of the receiving signal with time delay. In consideration of discrete sampling behavior, the sampling frequency can be expressed in the form of sequence data.

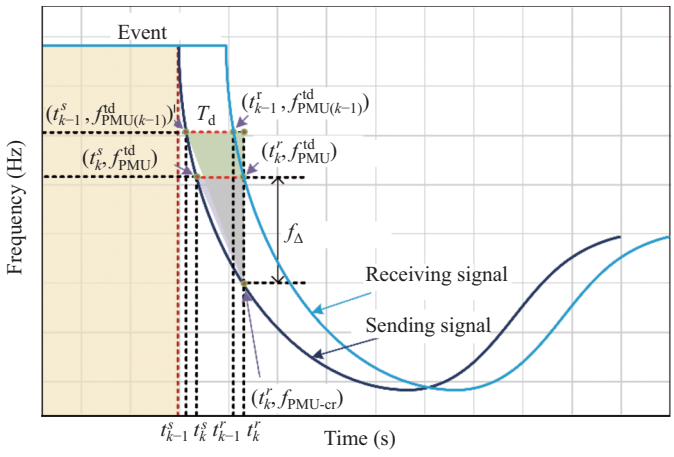

Fig. 4. The principle of time delay in frequency measurement.

As shown in Fig. 4, taking the k^{th} $(k = 1, 2, 3, \cdots)$ PMU reporting and transmission process as an example, $f_{\text{PMU}}^{\text{td}}$ arrived at the receiving time t_k^r, which is sent out at the sending time t_k^s. The time interval between t_k^r and t_k^s is the time delay T_d.

Due to the time delay, as shown in Fig. 4, when the signal $f_{\text{PMU}}^{\text{td}}$ arrives at the HVDC control, f_{PMU} has an additional change f_Δ. If the HVDC system adopts the $f_{\text{PMU}}^{\text{td}}$ as its control signal, the control performance of the HVDC system is inevitably reduced or even leads to severe contingency, because the HVDC system output may be insufficient or opposite from the system requirements. Therefore, the effect of the time delay must be considered in the HVDC system control process to guarantee the control precision.

In order to reduce the impact of control time delay on the HVDC system, a correction control strategy is proposed in this section.

The aim of the proposed time-delay correction control strategy is to correct the receiving frequency signal of the HVDC system so as to reduce the time interval between the actual frequency signal and the received frequency signal. In the 60 Hz system, the reporting frequency of PMUs in the actual application could be up to 120 Hz [36]. Thus, the rate of frequency change can be assumed unchanged between adjacent sampling points. For the $k-1^{\text{th}}$ and k^{th} sending points, the frequency changing rate ρ_k is written as:

$$\rho_k = \frac{f_{\text{PMU}}^{\text{td}} - f_{\text{PMU}(k-1)}^{\text{td}}}{t_k^s - t_{k-1}^s} \tag{18}$$

The estimation of the compensated frequency f_{com} can be calculated using ρ_k, the $k-1^{\text{th}}$ sending, and the k^{th} receiving points, expressed as:

$$f_{\text{com}} = \rho_k \cdot (t_k^r - t_{k-1}^s) \tag{19}$$

As a result, f_{com} is compensated based on $f_{\text{PMU}}^{\text{td}}$ to estimate the actual frequency deviation f_Δ, which can be written as:

$$f_\Delta = f_{\text{com}} - (f_{\text{PMU}}^{\text{td}} - f_{PMU(k-1)}^{\text{td}}) \tag{20}$$

Substituting (18), (19) into (20), then the corrected frequency can be expressed as:

$$f_{\text{PMU\_cr}} = f_{\text{PMU}}^{\text{td}} + \frac{f_{\text{PMU}}^{\text{td}} - f_{PMU(k-1)}^{\text{td}}}{t_k^s - t_{k-1}^s} \cdot (t_k^r - t_k^s) \tag{21}$$

As the principle described above, the time-delay correction control strategy is a model-free method that only relies on the frequency data, which is not impacted by the system operating conditions. The control diagram of the HVDC frequency control considering the proposed time-delay correction control strategy is shown in Fig. 5.

As shown in Fig. 5, the HVDC frequency control considering the proposed time-delay correction control strategy typically includes the following steps:

1) Step1: The frequency data is obtained from PMUs and then sent to PDCs. The function of the PDC is to process the data, such as bad data detection. After data processing, they will be sent to the HVDC frequency regulation control. In this paper, the frequency active power droop control is adopted as the HVDC frequency regulation control. It should be noted that other HVDC advancing frequency regulation control strategies could also be considered according to the operating requirements.

2) Step2: When the measured frequency data arrives at the HVDC frequency regulation control, these data will be sent to both the hold function and the time-delay correction control strategy. The objective of the hold function is to record the

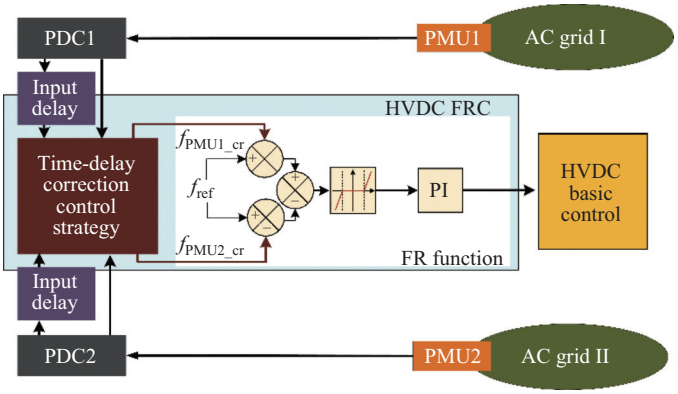

Fig. 5. The control diagram of the HVDC frequency control considering the proposed time-delay correction control strategy, where HVDC FRC is HVDC frequency regulation control and the FR function is frequency regulation function.

k^{th} timestamp and the corresponding frequency value. Then at the time of $k+1^{\text{th}}$, the hold function will send the k^{th} data to the time-delay correction control strategy for calculation. The time-delay correction control strategy will calculate the corrected frequency signal based on equation (21).

3) Step3: The corrected frequency data $f_{\text{PMU\_cr}}$ after calculation will be sent back to the frequency regulation function to perform active power compensation. The active power reference change will be reflected in the HVDC basic control.

It should be noted that the control strategy can be applied to any HVDC system with frequency regulation control.

IV. Analysis and Simulation Verification

A. Small Signal Analysis Considering Time-Delay Correction Control Strategy

In order to investigate the effectiveness of the proposed time-delay correction control strategy in system stability enhancement, the small signal test system in Section III is used again, with an additional time-delay correction control to be modeled.

Compared with the small signal state space model established in (17), the model with the time-delay correction control strategy takes (21) into account, which can be rewritten as:

$$f_{\text{PMU\_cr}} = f_{\text{PMU}}^{\text{td}} + \frac{f_{\text{PMU}}^{\text{td}} - f_{PMU(t-1)}^{\text{td}}}{T_s} \cdot T_d \tag{22}$$

where $f_{\text{PMU}(t-1)}^{\text{td}}$ can be considered as a series of signal delaying $f_{\text{PMU}}^{\text{td}}$ by one sampling period, which is expressed by a first-order delay loop:

$$f_{\text{PMU}(t-1)}^{\text{td}} = \frac{1}{1+sT_s} f_{\text{PMU}}^{\text{td}} \tag{23}$$

Then (23) can be written in the form of a differential equation as:

$$\frac{\text{d}}{\text{d}t} f_{\text{PMU}(t-1)}^{\text{td}} = \frac{1}{T_s} f_{\text{PMU}}^{\text{td}} - \frac{1}{T_s} f_{\text{PMU}(t-1)}^{\text{td}} \tag{24}$$

As expressed in (24), $f_{\text{PMU}(t-1)}^{\text{td}}$ contributes another state variable for the state space model. Therefore, the corrected frequency $f_{\text{PMU\_cr}}$ can be depicted with two state variables: $f_{\text{PMU}}^{\text{td}}$ and $f_{\text{PMU}(t-1)}^{\text{td}}$. By replacing $f_{\text{PMU}}^{\text{td}}$ in (3) with $f_{\text{PMU\_cr}}$, the input signal P_m of the outer loop control is expressed as:

$$P_m = (f_{\text{ref}} - f_{\text{PMU\_cr}}) \left(k_{\text{pf}} + \frac{k_{\text{if}}}{s}\right) + P_s \tag{25}$$

By linearizing (22), (24), (25), and combining (5), the small signal of P_m can be obtained,

$$\begin{aligned}\Delta P_m = {} & 40k_{\text{pf}} \left(\frac{1}{T_d} + \frac{1}{T_s}\right) \Delta z_1 \\ & + 1680k_{\text{pf}} \left(\frac{1}{T_d^3} + \frac{1}{T_s T_d^2}\right) \Delta z_3 - \frac{1}{2\pi} k_{\text{pf}} \left(1 + \frac{T_d}{T_s}\right) \Delta\omega_g \\ & + \left(k_{\text{pf}} \frac{T_d}{T_s} - k_{\text{if}} T_d\right) \Delta f_{\text{PMU}(t-1)}^{\text{td}} + k_{\text{if}} \Delta x_f + \Delta P_s\end{aligned} \tag{26}$$

So far, the overall small signal state space model considering the time-delay correction control strategy can be established as:

$$\frac{\text{d}\Delta \boldsymbol{x}_{\text{cr}}}{\text{d}t} = \boldsymbol{A}_{\text{cr}} \Delta \boldsymbol{x}_{\text{cr}} + \boldsymbol{B}_{\text{cr}} \Delta \boldsymbol{u} \tag{27}$$

where $\boldsymbol{A}_{\text{cr}}$ is a 14 × 14 state matrix while $\boldsymbol{B}_{\text{cr}}$ is a 14 × 2 input matrix. $\boldsymbol{x}_{\text{cr}} = [\delta,\ \phi_p,\ \phi_q,\ \phi_{\text{id}},\ \phi_{\text{iq}},\ \omega_g,\ z_1,\ z_3,\ x_f,\ f_{\text{PMU}(t-1)}^{\text{td}},\ z_2,\ z_4,\ \phi_p,\ \theta_p]^{\text{T}}$.

In Fig. 6, the eigenvalue locus of both $\boldsymbol{A}$ and $\boldsymbol{A}_{\text{cr}}$ are shown in the same complex plane. The eigenvalue sets of $\boldsymbol{A}$ in solid points were displayed in Fig. 3, with time delay T_d varying from 20 ms to 300 ms; while the star points refer to the eigenvalue sets of $\boldsymbol{A}_{\text{cr}}$, with the same range of T_d. As shown in Fig. 6(a), for $\boldsymbol{A}$ and $\boldsymbol{A}_{\text{cr}}$, the eigenvalues of their dominant modes both move to the positive direction of the real axis when T_d increases. However, the eigenvalue sets of the dominant mode of $\boldsymbol{A}_{\text{cr}}$ stay farther away from the imaginary axis, which means the system with a time-delay correction control strategy

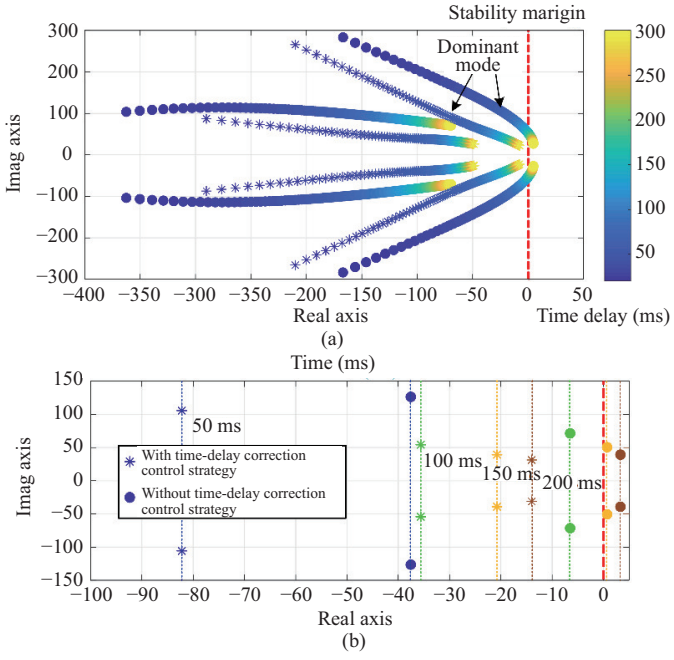

Fig. 6. The eigenvalue locus with varying time delay. (a) The eigenvalue locus with and without time-delay correction control strategy. (b) The eigenvalue of $\boldsymbol{A}$ and $\boldsymbol{A}_{\text{cr}}$ when time delay is 50 ms, 100 ms, 150 ms and 200 ms.

is more stable than the system without this control. To make the comparison more explicit, four groups of eigenvalues with time delays of 50, 100, 150, and 200 ms are shown in Fig. 6(b). For $\boldsymbol{A}$, when the time delay is chosen as 150 or 200 ms, which is larger than the boundary time delay 142 ms, the eigenvalues are located on the right half plane; while for $\boldsymbol{A}_{\mathrm{cr}}$, the eigenvalues have sufficient stability margins even with a time delay of 200 ms. It could be concluded from the small signal analysis that, the proposed time-delay correction control strategy has significant improvement in system stability.

B. Control Performance Verification in IEEE 39-Bus System

In order to test the performance of the proposed time-delay correction control strategy, a modified IEEE New England 39 bus system is studied in PSCAD/EMTDC, as shown in Fig. 7 [37].

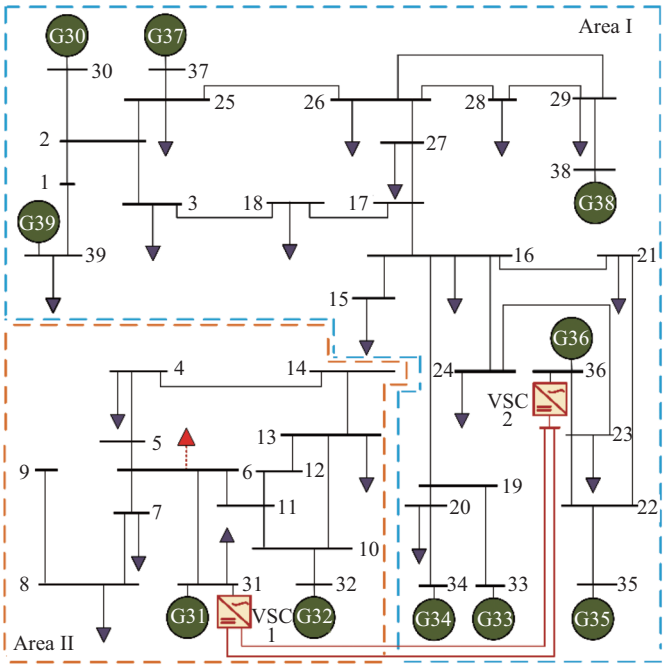

Fig. 7. Single-line diagram of a two-terminal VSC-HVDC system in a modified IEEE 39 bus system.

As shown in Fig. 7, the IEEE 39-bus system is divided into two asynchronous areas by disconnecting three AC interties: the AC interties 9–39, 3–4, and 14–15. The generators and the buses in the divided asynchronous areas are given in Table I. In the modified IEEE 39 bus system, a two-terminal VSC-HVDC system is embedded. The locations of the converter stations are as follows: VSC1 is connected to bus 31 and VSC2 is connected to bus 36. The parameters of the VSC-HVDC system are shown in Table II.

In the VSC-HVDC system, the VSC1 works at constant DC voltage control and VSC2 works at constant active power control. The frequency regulation control is configured at VSC2, with the proposed time-delay correction control strategy added. The initial power flow of the VSC-HVDC system is 30 MW from VSC1 to VSC2.

TABLE I
THE PARTITIONS OF TWO AREAS IN THE IEEE 39 BUS SYSTEM

Area	Generator	Bus
Area I	G30, G33, G34, G35, G36, G37, G38, G39	1, 2, 3, 7, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 33, 34, 35, 36, 37, 38, 39
Area II	G31, G32	4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 31, 32

TABLE II
MAIN PARAMETERS OF THE VSC-HVDC SYSTEM

Area	Items		Values
VSCs	Circuit parameters	Rated power	400 MW
		Rated DC voltage	400 kV
		Switching frequency	1350 Hz
	Control parameters	k_{pp}, k_{ip}	(0.001, 0.5)
		k_{pq}, k_{iq}	(0.0005, 0.5)
		k_{pid}, k_{iid}	(90, 10000)
		k_{piq}, k_{iiq}	(90, 10000)
		k_{pf}, k_{if}	(200, 0.5)
DC lines	Length of each DC line		100 km
	Resistance per unit length		0.01 Ω/km
	Inductance per unit length		0.85 mH/km
	Capacitance per unit length		0.013 μF/km

1) Performance Verification of the Proposed Time-Delay Correction Method

At time $t = 1.0$ s, the load at bus 6 increases 300 MW. Fig. 8 shows the comparison of three frequency signals: 1) the original frequency; 2) the time delayed frequency (150 ms time delay); 3) the time delayed frequency with the proposed correction control strategy (150 ms time delay).

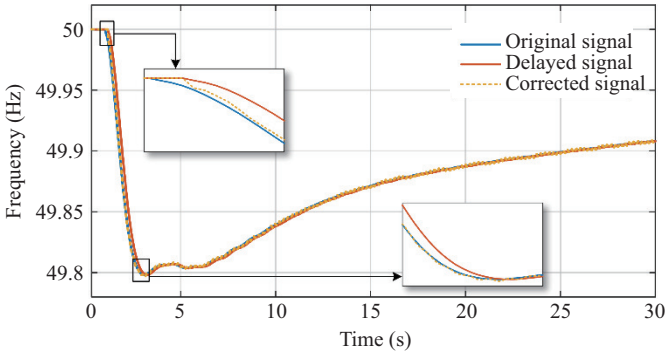

Fig. 8. Frequency comparison with and without proposed time-delay correction control strategy.

As shown in Fig. 8, the time delayed frequency lags behind the original frequency for 150 ms, especially obvious at the frequency drop process. At the beginning of the frequency drop, the corrected frequency first coincides with the delayed frequency. It is for the reason that the time-delay correction control collects delayed signals for calculation, so it only works when the delayed signal changes. The simulation results indicate that with a time-delay correction control strategy, the delayed frequency is corrected and the trend is similar to the original frequency, which proves the effectiveness of the proposed time-delay correction method.

2) Performance Verification of the Proposed Time-Delay Correction Control Strategy

In order to verify the effectiveness of the proposed time-delay control strategy, the frequency and active power at the VSC terminal are chosen to observe the system response with different inputs of frequency regulation controls. Three input signals are selected for comparison: 1) the original frequency f_{ori}; 2) the time delayed frequency f_{td}; 3) the time delayed frequency with the proposed correction control strategy, f_{cr}.

Case 1: At time $t = 1.0$ s, the load at bus 6 increases 300 MW; Time delay $T_d = 100$ ms.

Figure 9(a) shows the bus frequency at VSC2 with three different control input signals. With input signal f_{ori}, the bus frequency reaches its nadir around 49.80 Hz and then gradually restores to a new steady state. When the input signal is delayed as f_{td}, the bus frequency has a lower nadir of 49.79 Hz. In addition, small oscillation occurs during the frequency recovery, which proves the influence of time delay on the small signal stability in Section III. After f_{td} is corrected with f_{cr}, the bus frequency is close to that with f_{ori} as the input signal. The frequency nadir becomes higher and oscillation disappears.

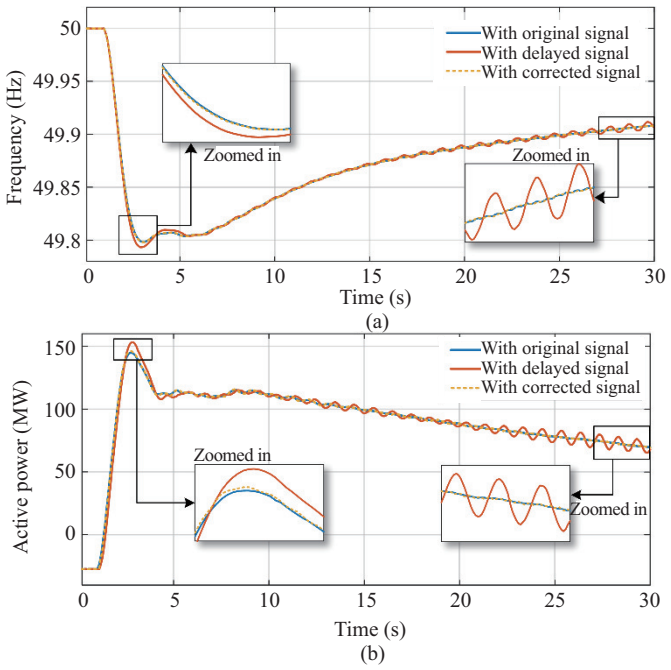

Fig. 9. Control effect comparison when $T_d = 100$ ms. (a) The frequency comparison. (b) The active power comparison.

The control effect can also be observed in active power at VSC2. As shown in Fig. 9(b), with input signal f_{ori}, the maximum of active power transmission from VSC1 to VSC2 is 144.8 MW; while with delayed input signal f_{td}, the active power reversal compensation can be up to 153.3 MW. After f_{td} is corrected with f_{cr}, the highest active power support is 146.1 MW, which is close to that with input signal f_{ori}. Moreover, the active power with the delayed input signal has an oscillation in the restoration process, which is not observed with the other two input signals.

Case 2: At time $t = 1.0$ s, the load at bus 6 increases 300 MW; Time delay $T_d = 150$ ms.

With a larger time delay, the results are clearer for comparison. As can be seen in Fig. 10(a), the bus frequency nadir at VSC2 is 49.80 Hz, 49.79 Hz, and 49.80 Hz with the input signals of f_{ori}, f_{td}, f_{cr} respectively. During the recovery process, the bus frequency with input signal f_{td} has a more obvious oscillation compared to Case 1, which also confirms the conclusion in Section III: the increase of time delay could reduce the small signal stability margin and even cause system instability. With f_{cr} as the input signal, the bus frequency can be close to that with input signal f_{PMU}, so it can be summarized that the time-delay correction control strategy can improve the frequency nadir and enhance the system stability.

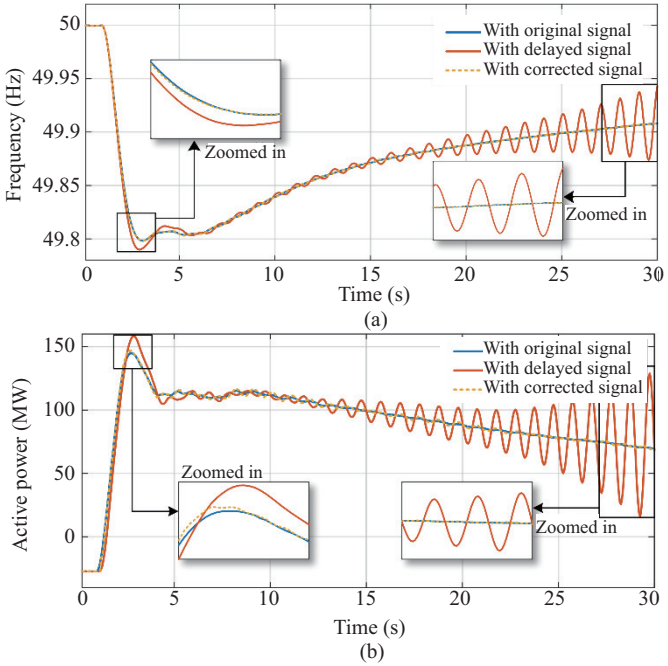

Fig. 10. Control effect comparison when $T_d = 150$ ms. (a) The frequency comparison. (b) The active power comparison.

In Fig. 10(b), the maximum of active power reversal compensation is 144.8 MW, 158.3 MW, and 146.9 MW with the input signals of f_{ori}, f_{td}, f_{cr} respectively. Similarly, there is a large oscillation when the input signal is delayed, but the system stays stable with f_{ori} orf_{cr} as input. Therefore, the issue of increased power compensation and system instability caused by the time delay can be resolved by the proposed correction control strategy.

Case 3: In order to simulate a situation closer to the real project, the randomness in time delay should be considered. The time delay is not a fixed value and can be assumed to satisfy the normal distribution, which is represented as:

$$T_d \in N(\mu, \sigma^2) \tag{28}$$

where μ is the average value and σ^2 is the variance value for the normal distribution. In this case, $\mu = 100$ ms $, \sigma^2 = 10$ ms.

At time $t = 1.0$ s, the load at bus 6 increases 300 MW.

Figure 11(a) shows the bus frequency at VSC2 and that the input signals f_{td} and f_{cr} have a random time delay. With input signal f_{cr}, the frequency nadir becomes higher than that with input signal f_{td}, which is closer to the original frequency nadir. In the recovery process, although the frequency with input signal f_{cr} restores a bit slower than the original case, the oscillation coming from the delayed signal disappears. Thus, it can be concluded that the time-delay corrected control strategy is still effective with a random time delay.

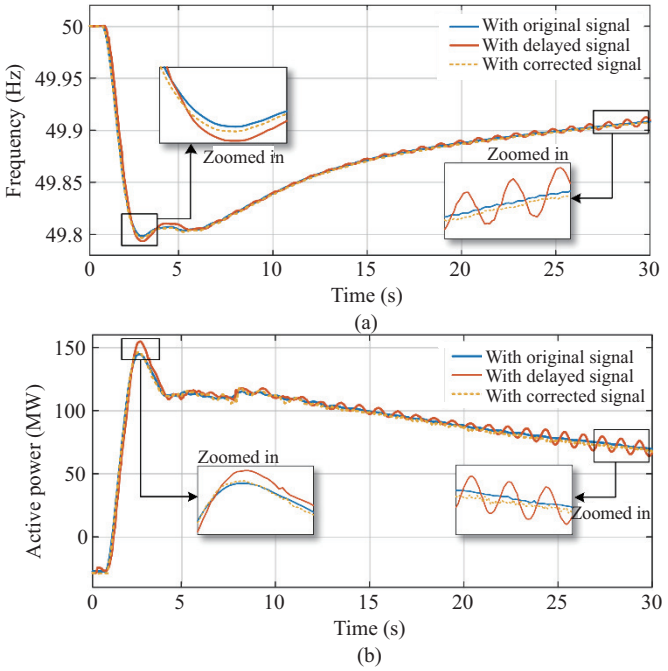

Fig. 11. Control effect comparison when $T_d \in N(\mu, \sigma^2)$, $\mu = 100$ ms, $\sigma^2 = 10$ ms. (a) The frequency comparison. (b) The active power comparison.

For active power comparisons, Fig. 11(b) shows similar conclusions. The maximum power reversal compensation with the three input signals f_{ori}, f_{td} and f_{cr} is 144.8 MW, 154.8 MW, and 146.6 MW, respectively. In addition, the stability issue still exists when the input signal has a random time delay. After the input signal is corrected, the active power is close to the original case and the system stability is improved.

V. Conclusion

In this paper, a time-delay correction control strategy for HVDC frequency regulation service is proposed to suppress the time-delay influence. In order to analyze the impact of time delay on HVDC control, first, a small signal model is conducted. Then, according to the cause of the time delay, a time-delay correction control strategy for HVDC frequency regulation control is proposed. The proposed time-delay correction control is verified in both the established small signal model and the modified IEEE 39 bus system. The small signal analysis shows that the system with a time-delay correction control strategy has more stability margin than the system without this control. The simulation results in the modified IEEE 39 bus system indicate that the proposed time-delay correction control strategy could improve the frequency nadir and enhance system stability.

A future study includes (1) an application of the time-delay correction control strategy to a hybrid HVDC system. (2) improvement of the time-delay correction control method to make it adaptive to noisy frequency data.

Appendix

State Matrices of the System

$$\boldsymbol{A} = \begin{bmatrix}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & & & & & & & & & 0 & 0 & 0 & 0 \\
0 & -K_{22}m_2K_{31} & & -K_{22}m_2 & & -K_{22}m_2K_1K_{21}K_{31}+K_{22}K_1 & & & & & & & \\
0 & & & & & & & & & 0 & 0 & 0 & 0 \\
0 & -K_{32}K_{21}m_2K_{31} & & -K_{32}K_{21}m_2 & & (-K_{32}K_{21}m_2-K_{32}m_3) & & & & 0 & 0 & 0 & 0 \\
0 & -K_{32}m_3K_{31}+K_{32} & & -K_{32}m_3 & & \cdot K_1K_{21}K_{31}+K_{32}K_{21}K_1 & & & & 0 & 0 & 0 & 0 \\
0 & m_1N^{-1}K_{31} & & m_1N^{-1} & & m_1N^{-1}K_1K_{21}K_{31} & & & & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{2\pi} & -\frac{20}{T_d} & -\frac{840}{T_d^3} & 0 & -\frac{180}{T_d^2} & -\frac{1680}{T_d^4} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -\frac{1}{2\pi} & \frac{40}{T_d} & \frac{1680}{T_d^3} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & & & & & & & & & 0 & 0 & 0 & 0 \\
0 & K_4N^{-1}K_{31} & & K_4N^{-1} & & K_4N^{-1}K_1K_{21}K_{31} & & & & & & & \\
0 & & & & & & & & & 0 & 0 & 1 & 0
\end{bmatrix}$$

$$\boldsymbol{A}_{cr} = \begin{bmatrix}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & & & & & & & & & & 0 & 0 & 0 & 0 \\
0 & -K_{22}m_2K_{31} & & -K_{22}m_2 & & -K_{22}m_2K_1'K_{21}K_{31}+K_{22}K_1' & & & & & & & & \\
0 & & & & & & & & & & 0 & 0 & 0 & 0 \\
0 & -K_{32}K_{21}m_2K_{31} & & -K_{32}K_{21}m_2 & & (-K_{32}K_{21}m_2-K_{32}m_3) & & & & & 0 & 0 & 0 & 0 \\
0 & -K_{32}m_3K_{31}+K_{32} & & -K_{32}m_3 & & \cdot K_1'K_{21}K_{31}+K_{32}K_{21}K_1' & & & & & 0 & 0 & 0 & 0 \\
0 & m_1N^{-1}K_{31} & & m_1N^{-1} & & m_1N^{-1}K_1'K_{21}K_{31} & & & & & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{2\pi} & -\frac{20}{T_d} & -\frac{840}{T_d^3} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{180}{T_d^2} & -\frac{1680}{T_d^4} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -\frac{1}{2\pi} & \frac{40}{T_d} & \frac{1680}{T_d^3} & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{T_s} & -\frac{1}{T_s} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & & & & & & & & & & 0 & 0 & 0 & 0 \\
0 & K_4N^{-1}K_{31} & & K_4N^{-1} & & K_4N^{-1}K_1'K_{21}K_{31} & & & & & & & & \\
0 & & & & & & & & & & 0 & 0 & 1 & 0
\end{bmatrix}$$

In the matrices, the defined elements are as follows:

$$A_1 = -\frac{1}{\omega_0 T_J}[i_{\mathrm{sd0}} \quad i_{\mathrm{sq0}}],\ A_2 = -\frac{1}{\omega_0 T_J}[E'_{d0} \quad E'_{q0}]$$

$$\boldsymbol{a} = [0 \quad -1/X_f;\ -1/X_f \quad 0]$$

$$\boldsymbol{b} = \frac{3}{2} \cdot \begin{bmatrix} i_{\mathrm{sd0}} & i_{\mathrm{sq0}} \\ i_{\mathrm{sq0}} & -i_{\mathrm{sd0}} \end{bmatrix},\ \boldsymbol{c} = \frac{3}{2} \cdot \begin{bmatrix} u_{\mathrm{sd0}} & u_{\mathrm{sq0}} \\ -u_{\mathrm{sq0}} & u_{\mathrm{sd0}} \end{bmatrix}$$

$$\boldsymbol{d} = \begin{bmatrix} -R_{\mathrm{a}} & -X_d \\ X_d & -R_{\mathrm{a}} \end{bmatrix}$$

$$\boldsymbol{K}_1 = \begin{bmatrix} -\frac{k_{\mathrm{pf}}}{2\pi} & \frac{40k_{\mathrm{pf}}}{T_d} & \frac{1680k_{\mathrm{pf}}}{T_d^3} & k_{\mathrm{if}} \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\boldsymbol{K}_1' = \begin{bmatrix} -\frac{k_{\rm pf}}{2\pi}\left(1+\frac{T_d}{T_s}\right) & 0 \\ 40k_{\rm pf}\left(\frac{1}{T_d}+\frac{1}{T_s}\right) & 0 \\ 1680k_{\rm pf}\left(\frac{1}{T_d^3}+\frac{1}{T_sT_d^2}\right) & 0 \\ k_{\rm if} & 0 \\ \frac{k_{\rm pf}T_d}{T_s}-k_{\rm if}T_d & 0 \end{bmatrix}^{\rm T}$$

$$\boldsymbol{K}_{21} = [k_{\rm pp} \;\; 0; \;\; 0 \;\; k_{\rm pq}],\; K_{22} = [k_{\rm ip} \;\; 0; \;\; 0 \;\; k_{\rm iq}]$$

$$\boldsymbol{K}_{31} = [k_{\rm pid} \;\; 0; \;\; 0 \;\; k_{\rm piq}],\; K_{32} = [k_{\rm iid} \;\; 0; \;\; 0 \;\; k_{\rm iiq}]$$

$$\boldsymbol{K}_4 = [0 \;\; k_{ipll}; \;\; 0 \;\; k_{\rm ppll}]$$

$$\boldsymbol{M}_1 = \begin{bmatrix} \frac{3u_{\rm cqo}-3i_{\rm sd0}X_f}{2X_f} & \frac{2u_{s0}-3u_{\rm cdo}-3i_{\rm sq0}X_f}{2X_f} \\ \frac{-2u_{s0}+3u_{\rm cdo}-3i_{\rm sq0}X_f}{2X_f} & \frac{3u_{\rm cqo}+3i_{\rm sd0}X_f}{2X_f} \end{bmatrix}$$

$$\boldsymbol{M}_2 = \begin{bmatrix} \frac{3u_{\rm cqo}}{2X_f} & \frac{2u_{c0}-3u_{\rm cdo}}{2X_f} \\ \frac{2u_{c0}+3u_{\rm cdo}-4u_{s0}}{2X_f} & \frac{3u_{\rm cqo}}{2X_f} \end{bmatrix}$$

$$u_{s0} = 1.5(u_{\rm sd0}^2+u_{\rm sq0}^2),\; u_{c0} = 1.5(u_{cd0}^2+u_{cq0}^2)$$

$$\boldsymbol{M}_3 = \begin{bmatrix} \frac{3k_{\rm pp}k_{\rm pid}i_{\rm sd0}}{2} & \frac{3k_{\rm pp}k_{\rm pid}i_{\rm sq0}}{2} \\ \frac{3k_{\rm pq}k_{\rm piq}i_{\rm sq0}}{2} & -\frac{3k_{\rm pq}k_{\rm piq}i_{\rm sd0}}{2} \end{bmatrix}$$

$$\boldsymbol{M}_4 = \begin{bmatrix} \frac{3k_{\rm pp}k_{\rm pid}u_{\rm sq0}}{2X_f} & \frac{-3k_{\rm pp}k_{\rm pid}u_{\rm sd0}-3k_{\rm pid}}{2X_f} \\ \frac{3k_{\rm pq}k_{\rm piq}u_{\rm sd0}+3k_{\rm piq}}{2X_f} & \frac{3k_{\rm pq}k_{\rm piq}u_{\rm sq0}}{2X_f} \end{bmatrix}$$

$$N = M_3 + M_4(I - M_1^{-1}M_2)$$

$$m_1 = A_1 I + (A_2 - A_1 d)a(I - M_1^{-1}M_2)$$

$$m_2 = [b + ca(I - M_1^{-1}M_2)N^{-1}]$$

$$m_3 = a(I - M_1^{-1}M_2)N^{-1}$$

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